# CS 286 Two Lecture Introduction

# Parallel Processing: A Hardware Solution & A Software Challenge

#### We're on the Road to Parallel Processing





#### Hardware Solution (Day 1)

### Software Challenge (Day 2)

#### Opportunities



# Hardware Solution Technical



# Opportunities Technical



### Hardware Solution

- Technical
- Business
- Software Challenge
  - Technical
  - Business

### Opportunities

- Technical
- Business

### Outline

### Hardware Solution

- Technical
- Business
- Software Challenge

### Opportunities

## Hardware Solution - Technical **Evolution of Computer Architectures**

#### **Computer Hardware Evolution Highway**

Car

&







Macro





Intel 8086		tel Core 2 Duo
1978	Year	2006
29,000	Transistors	291,000,000
5 MHz	<b>Clock Frequency</b>	2.9 GHz

In 28 Years from 1978 to 2006:

- Number of Transistors Increased 10,034X
- Clock Frequency Increased 586X

Primary Driver / Facilitator was (and is) Moore's Law:

- Number of Transistors Doubles every 18-24 Months
- Stated by Gordon Moore, Intel Co-Founder in 1965
- Prediction has been proven valid over a long term
  - "Prediction" has been the "Law" for over 40 years







Huge Clock Frequency Increases

Unfortunately .....

#### **Clock Rate Limits Have Been Reached**



Source: Patterson, Computer Organization and Design



Intel Developer Forum, Spring 2004 - Pat Gelsinger

Hardware Solution - Technical **Evolution of Computer Architectures** Micro-Scopic View Power (and Heat) Grows as Frequency<sup>3</sup> Power  $\propto$  Voltage<sup>2</sup> x Frequency Voltage  $\propto$  Frequency Power  $\propto$  Frequency<sup>3</sup> • How can HW Performance Continue to Increase? Single Core Multi-Core



Instruction-Level Parallelism (ILP) was also Heavily Used Implemented On-Chip via Hardware

Transparent to Software (No impact on Programmers)

We will Study Two Types: Pipelining (Intra-Instruction Parallelism) Multi-Function Units (Inter-Instruction Parallelism)

ILP has provided reasonable speedups in the past, Unfortunately.....

#### Instruction-Level Parallelism Limits have been Reached too





Clock Frequency Scaling Limits have been Reached

- Instruction Level Parallelism Limits have been Reached
- Era of Single Core Performance Increases has Ended
- No More "Free Lunch" for Software Programmers
   Multiple Cores Will Directly Expose Parallelism to SW
- All Future Micro-Processor Designs will be Multi-Core
   Evident in Chip Manufacturer's RoadMaps

#### Hardware Solution - Technical **Evolution of Computer Architectures** Micro-Scopic View Summary Intel Multi-core Roadmap 2005 2006 2007 Future Platform Tukwila Poulson Itanium® Itanium® 2 Processor Montecito Montvale. processor Dimona thion Intel<sup>®</sup> Xeon<sup>®</sup> Intel® Xeon<sup>6</sup> Tigerton Dunnington MP Server Tulsa processor MP processor MP Intel® Xeon® processor DP Server / Intel® Xeon® Clovertown Dempsev Woodcrest ws Processor w/ 2MB Future cache Sossaman UP Server / Kentsfield Pentium<sup>®</sup> Processor Power 5 WS Pentium® D Extreme Edition Future Conroe Desktop (Presler) Client Pentium® D Intel Core™ Merom Future Pentium<sup>®</sup> M processor Mobile Duo Client solaris Multi-core Multi-core Single intel ULTRASPARC Refer to 'fact sheet' for All products and dates are preliminary and core (>=2 cores) (>=4cores) subject to change without notice specific product timings



It will be used to Increase Number of Cores Instead





## Hardware Solution - Technical Evolution of Computer Architectures

#### Computer Hardware Evolution Highway

Macro





Personal Computer Nodes: 1 Location: Desktop



Cluster Computer Nodes: 10's – 100's Location: Local



Example Cluster Computer









Cloud Computer Nodes: 10,000's Location: Highly Distributed





#### Single Node

**Sequential Processing** 



Many Nodes

**Parallel Processing** 

## Hardware Solution - Business Evolution of Computer Architectures

















#### **Key Points**

#### Hardware Solution

Parallel Processing is really an Evolution in

- Micro- and Macro-Architecture Hardware
  - That provides a Solution to:
    - The Heat and Power Wall
    - The Limitations of ILP
    - Cost-Effective Higher Performance

Parallel Processing is also a Software Challenge