EE 172

DR RAY KWOK

AMPLIFIER PROJECT

BY

AMPLIFIER GROUP

05/25/04

AC Analysis Group	**DC Analysis Group**	**S-Parameter Analysis and Layout Group**	
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Kenneth Tseng	Rajan Joshi	Venkata Vegesna	

Introduction

Design Background

The class project required to build a transmitter and receiver circuit. The specific task that this group was to design for the project is the amplifier. The amplifier is the block in the transmitter and receiver circuit that takes a signal and amplifies to a desired level so that other successive block can utilize the signal.

The transmitter block requires the amplifier to have the following major specifications:

- Input/output impedance 50Ω
- Power Gain 27-30dBm
- Operating Frequency 915MHz±50MHz
- Gain Flatness ±1dB

The receiver block requires a Low Noise Amplifier (LNA) to have the following major specifications:

- Input/output impedance 50Ω
- Power Gain 27-30dBm
- Operating Frequency 915MHz±50MHz
- Gain Flatness ±1dB
- Noise Figure 1dB Max

The receiver block LNA is beyond the scope of this project since the design of this amplifier requires more investigation than time can permit for this course. Therefore, the amplifier designed for the transmitter stage will be used in lieu of the LNA. The transmitter amplifier specification for the power gain requires that a two-stage amplifier be designed. Again, the design of such an amplifier requires investigation and time to successfully complete the project. So, a single stage amplifier with a maximum power gain of 15dBm will be designed. The aim was to successfully verify the single stage prototype circuit. Once successfully verified, a second duplicate prototype circuit will be made for the transmitter.

Design Introduction

The design of an amplifier requires proper DC biasing for maximum gain, AC analysis to determine bandwidth and voltage gain, S-parameter analysis for transistor stability and two-port matching, and layout analysis.

A decision was made to design a simple class A amplifier. Once considering all the above items, a single stage class A design was implemented and built on a board. The design was tested as much as time permitted. A duplicate board was not built since the testing was not completed.

The report format of the design steps are presented in the following order (author/s in parenthesis):

- Board Layout (Venkata Vegesna)
- DC biasing Analysis (Rajani Joshi, Mai Cao)
- AC Analysis (Kenneth Tseng, Hadi Alamdar)
- S-Parameter Analysis (Adesoji Sajuyigbe, LiCheng Shiue, Venkata Vegesna)

- Amplifier Testing
- Discussion/Conclusion

Board Layout (Ven)

The board layout requires that the trace width on board is equivalent to a 50Ω-transmission line. A software application named APPCAD made by Agilent was used to determine the trace width. An assumption was made that the software utilizes the equations in (Pozar, 162) for the calculation of the trace width required to achieve 50Ω. The following parameter were entered into APPCAD:

- εr=4.6 (FR-4)
- Thickness of trace=1mil
- Height=62.5mil
- Frequency=915MHz

The width of the trace was varied to achieve a 50Ω-transmission line. The thickness was calculated to be 0.115in. When the trace tested to measure the S11 on the network analyzer, the impedance was 68Ω. The trace was increased in width to 0.168in. to make a 50Ω-transmission line.

DC Biasing Analysis (Rajani, Mai)

DC ANALYSIS FOR N-MOSFET CIRCUITS:

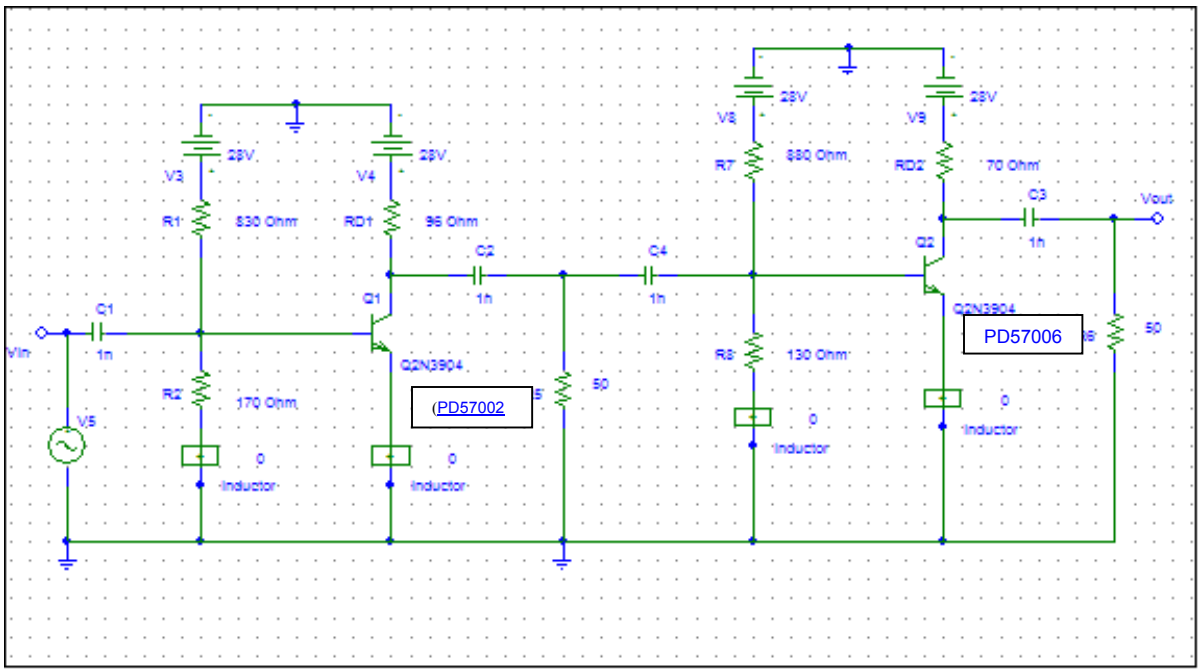


Figure 1: Schematic for Two Stage Amplifier Circuit for 30 dB Gain

1) For PD57002

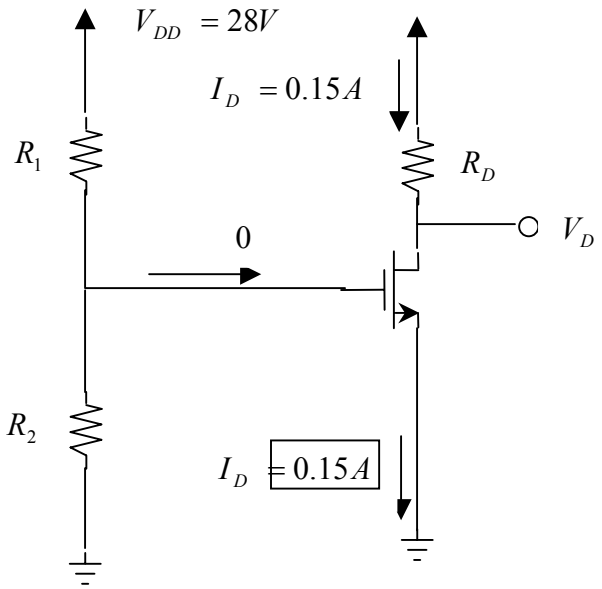


Figure 2: DC analysis circuit for PD57002 and PD57006

The saturation region is used if the FET is to operate as an amplifier.

Therefore,

$$V_{DS} \geq V_{GS} - V_T$$

Where,

V_{DS} : Drain source voltage

V_{GS} : Gate source voltage

V_T : Threshold voltage

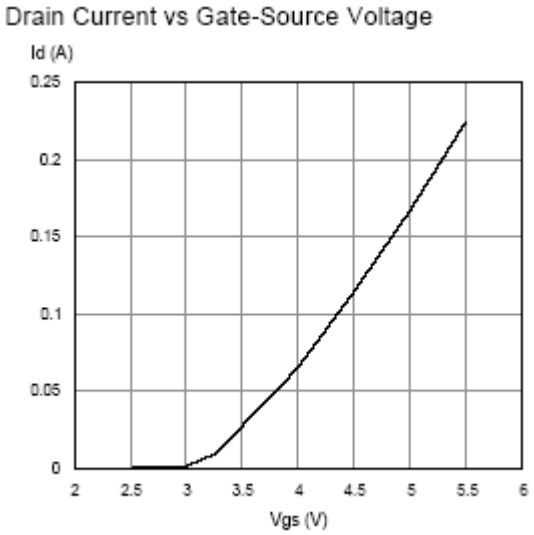


Figure 3: Vd Vs Vg curve for PD57002

$V_{GS_=} = 4.8V$ (From graph 1of Drain Current & Gate Source

$V_T := 3\text{V}$ Voltage in the data sheet of PD57002)

$V_{DS} = 13.5V$ (From data sheet of PD57002)

For n-channel enhancement-type MOSFET operates in the saturation region when V_{GS} is greater than V_T and the value of V_T is controlled during device fabrication and typically lies in the range 1 to 3V .Therefore, we chose $V_T = 3V$.

$\Rightarrow$ $13.5V \geq (4.8V - 3V = 1.8V)$ (It does make physical sense)

The required value for R_D can be found as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

Since the source voltage is connect to ground $\Rightarrow V_{DS} = V_D = 13.5V$

$$R_D = \frac{28V - 13.5V}{150mA} = 96\Omega$$

To find the values required for R_1 & R_2, we are used the application of voltage divider.

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}\ (\ V_G = V_{GS} = 4.8V \text{ since } V_s = 0V)$$

$$\Leftrightarrow \quad 4.8V = 28V\frac{R_2}{R_1 + R_2}$$

or $$\frac{4.8V}{28V} = \frac{R_2}{R_1 + R_2}$$

$$0.17R_1 + 0.17R_2 = R_2$$

$$0.17R_1 = 0.83R_2$$

Taking the above ratio $\Rightarrow R_1 = 830K\Omega \ \& \ R_2 = 170k\Omega$

2) For PD57006

$V_{DS} = 13.5V$ (From data sheet of PD57002)

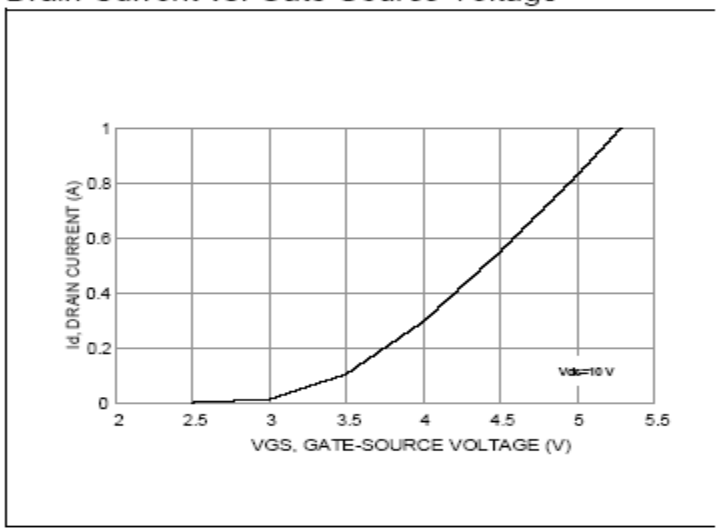


Figure 3: Vd Vs Vg curve for PD57006

$V_{GS\_} = 4.8V$ (From graph of Drain Current & Gate Source Voltage in the data sheet of PD57006)

V_T : 2.5 V

$\Rightarrow$ 13.5 > (3.56- 2.5= 1.06 V)

The required value for R_D can be found as follows:

Since the source voltage is connect to ground $\Rightarrow V_{DS} = V_D = 13.5V$

$$R_D = \frac{28\text{-}13.5}{200\text{mA}} = 72.5\Omega$$

To find the values required for R_1 & R_2, we are used the application of voltage divider.

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2} \text{ (Since } V_G = V_{GS} = 3.65V,\ V_s = 0V)$$

$$3.65 = 28\ \frac{R2}{R1 + R2}$$

$$0.130\ R1 = 0.\ 869R2$$

Taking above ration: R1= 870KΩ; R2= 130KΩ

PROBLEM AND SOLUTION:

PROBLEM	SOLUTION
1. Calculating the values of Rd, R1 and R2 to design an amplifier	- With careful study of the datasheet of the transistor the all available and usable information were extracted. - Seek help from Professor Zoroofchi, Javad
2. Finding the exact resistors value and power dissipated in stores	- Used the closest possible value we can find
3. After soldering the part in the board, difficulty in getting the desired values of Vds and Vgs when the board was tested	- Used a spare transistor and tested in the breadboard (without soldering). - After the circuit gave the required values for Vgs, Vds, the circuit was transferred to the soldering board. - A register and the MOSFET soldered were found faulty

AC Analysis (Kenneth, Hadi)

AC Analysis for PD57002

AC Analysis for PD57006
Cc1=Cc2=100uF

s^2, two zeros at zero frequency

$$\mathrm{R_{C1}} = R_S + R_1 // R_2$$

$$\mathrm{R_{C1}} = 50 + 839k // 170k = 141k\Omega$$

$$\omega_{P1} = \frac{1}{C_{C1}R_{C1}}$$

$$\omega_{P1} = \frac{1}{10\times10^{-6}\times141\times10^{3}} = 0.7rad/s$$

$$\mathrm{R_{C2}} = 96 + 50 = ; 150\Omega$$

$$\omega_{P2} = \frac{1}{C_{C2}R_{C2}}$$

$$\omega_{P2} = \frac{1}{10\times10^{-6}\times150} = 666rad/s$$

$$f_{p2} = 106Hz$$

$$\frac{V_o}{V_g} = -\frac{R_L^{'}}{1/g_m} = -g_m R_L^{'}$$

$$\frac{V_g}{V_s} = \frac{141k}{R_s + 141k} \; ; 1$$

$$\frac{V_o}{V_s} \; ; -g_m R_L^{'}$$

$$C_T = C_{gs} + C_m = C_{gs} + C_{gd}(1 + g_m R_L^{'})$$

$$\omega_{P3} = \frac{1}{C_T R_T},\ \mathrm{R_T} = 141 // R_s\ ;\ R_s$$

$$\omega_{P4} = \frac{1}{C_{gd} R_{eq4}},\ \mathrm{R_{eq4}} = 50 // 96$$

$$\omega_{P3} = \omega_{P4}$$

AC Analysis to meet 915MHz for PD57006S

$$R_{C1} = \frac{(880k)(130k)}{880k + 130k} = 113.3k\Omega$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.2}{3.55 - 2.5} = 0.38095\frac{A}{V}$$

$$\omega_{P1} = \frac{1}{C_{C1} R_{C1}} = \frac{1}{(10 \times 10^{-6})(113.3k)} = 0.883 rad/s$$

$$R_{C2} = 73 + 50 = 123\Omega$$

$$\omega_{P2} = \frac{1}{C_{C2} R_{C2}} = \frac{1}{(10 \times 10^{-6})(123)} = 813 rad/s$$

The gain fro the circuit is found on midband frequency

$$R_L^{'} = R_D // R_L$$

$$\frac{V_o}{V_g} = -\frac{R_L^{'}}{1/g_m}$$

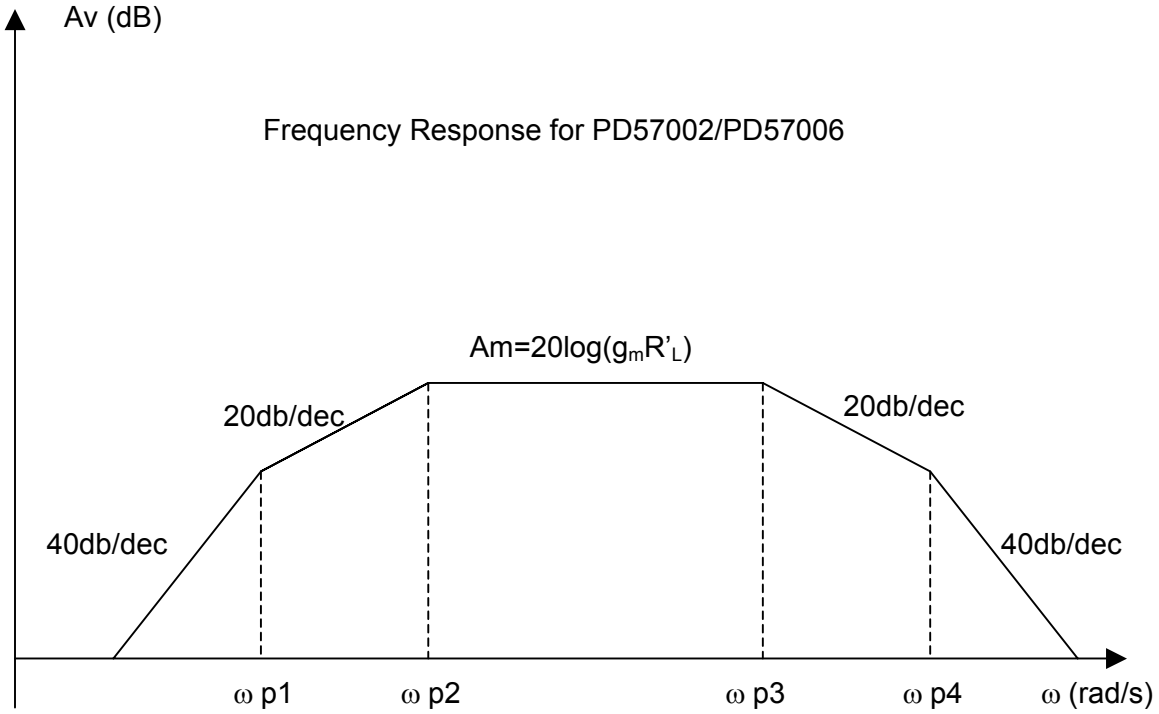
$$= -g_m R_L^{'}$$

$$= -g_m \frac{R_D R_L}{R_D + R_L}$$

$$= 0.38095 \times 29.67$$

$$= 11.3$$

$$\text{in dB} \Rightarrow \frac{V_o}{V_g} = 21.06 dB$$


Av (dB)
Frequency Response for PD57002/PD57006
Am=20log(gmR'L)
20db/dec
20db/dec
40db/dec
40db/dec
ω p1
ω p2
ω p3
ω p4
ω (rad/s)

S-Parameter Analysis (Soji, Li, Ven)

Matching

In the design of an amplifier, a major practical consideration is matching. Matching is needed in order to minimize signal reflections to and from the ports. At higher frequencies, matching is more crucial than at lower frequencies. In this design of a 915MHz RF amplifier, the matching is significantly important. At this frequency, the effects of a mismatch often result in energy loss.

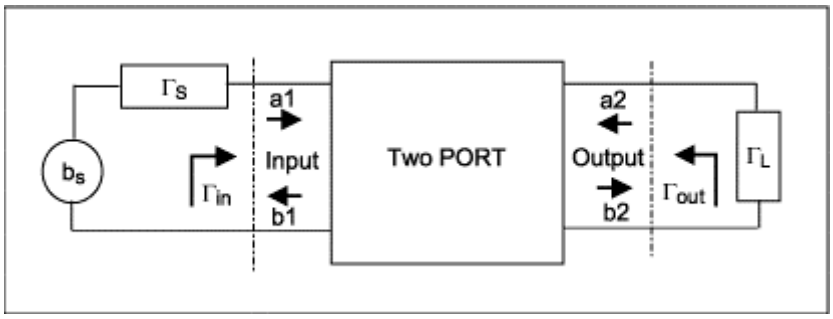


Figure 1: Two Port System
(Courtesy: maxim-ic.com)

Conjugate Matching

In a multi-port network, simultaneous matching should be employed. Simultaneous matching involves matching one port in the network while taking the other port(s) into consideration. Using this matching technique, each port is conjugately matched to other ports in the system. In this design, the amplifier – a two port network – is matched using conjugate matching. The equations from 3.6.1 to 3.6.8 (G. Gonzalez, pg. 240) show the procedures of obtaining perfect matching parameters. A visual description (Signal Flow Graph) of the S-matrices in a two port network is illustrated in Figure 2 below.

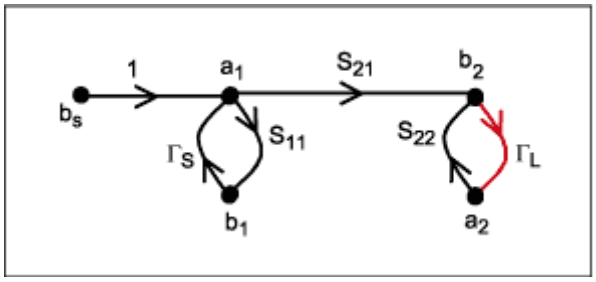


Figure 2: S-parameters
(Courtesy: maxim-ic.com)

In order to use the conjugate matching equations, the Rollett stability factor, K, has to be greater than unity (G. Gonzalez, 226, 241). The expression for K is given in the equation below.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \text{ where } \Delta = S_{11}S_{22} - S_{12}S_{21}$$

Based on the S-parameter specifications given for the PD57002 transistor at 900MHz, the value of K calculated is 0.148 which is much less than 1. As a result, the conjugate matching method cannot be applied at this point.

Stability

As stated above, for unconditionally stable, K must be greater than unity. On the contrary, when K is less than unity, the transistor is potentially unstable.
Since the S-parameters of the PD57002 result in a value of K = 0.148, the transistor is potentially unstable.

The methods that could be engaged to stabilize this transistor are resistive loading or adding negative feedback (G. Gonzalez, 228). Resistive loading is chosen instead of adding negative feedback because of its simplicity. In this case, there are four types of resistive loading that could help to improve stability (G. Gonzalez, 228). A series resistor implemented at the input of the transistor is used to stabilize the amplifier discussed in this report.

The required value for a stabilizing resistor can be computed when the stability circles are drawn on a Smith Chart. The equations 3.3.7 to 3.3.10 (G. Gonzalez, 218) show the formulas required to get the radius and center of the load and source stability circles respectively. Once the stability circles are drawn on the Smith Chart, the stable region can be determined. The stable region is the area on the Smith Chart that is not enclosed by the stability circles.

It is important to avoid the region of overlap between the stability circle and the Smith Chart because this region dictates instability. For this reason, the stability circle(s) should be moved out of the Smith Chart. To move these stability circle(s) away, any impedance or admittance circle tangent to the stability circle(s) should be traced to the real axis. The value at the intersection with the real axis is the normalized value of the stabilizing impedance (G. Gonzalez, 227). Since the trace follows the impedance chart, the resistive value obtained will be series to the gate/drain of the transistor.

For the PD57002 transistor, a stabilizing impedance of 10 Ω is determined. Thus, a 10 Ω resistor is chosen to be connected in series with the gate of the transistor. The new S-parameter values of the transistor block are then computed (G. Gonzalez, 228). The computation is a simple process of cascading the resistor with the transistor. The resistor and transistor parameters are converted to ABCD parameter. Both ABCD parameters are multiplied and a new ABCD matrix is calculated. The new ABCD matrix is then converted S parameters. The newly calculated S parameters are used to calculate the new K value. The new K value is 1.102. Since K>1, the transistor/resistor combination is considered unconditionally stable. The new S parameters can be used to conjugately match the transistor.

	Unstabilized	Stabilized (with 10 Ω)
K	0.148	1.1
S11	-0.753 – j0.489	-0.506 – j0.354
S21	2.268 + j1.709	1.987 + j1.372
S12	0.023 – j0.021	0.022 – j0.019
S22	-0.563 – j0.696	-0.048 – j0.696

Table 1: Comparison of parameters before and after resistive loading

With the new S-parameters and calculated reflection coefficients, the matching is done using a Smith Chart.

Matching (input/output)

to be discussed

After the values and configuration of the matching network is obtained, the realization of the matching is simulated using Microwave Office (MWO). While doing the simulation in MWO, the values of the matching lumped elements are tuned to optimize the performance. The tuned schematic is shown in Figure 3, and the S-parameters versus frequency plot is shown in Figure 4. Table 2 shows expected S-parameters of the whole amplifier system a

Test Results

Discussion/Conclusion