2.4GHz Microwave Power Amplifier

By

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Abstract:

Microwave power amplifiers are used to boost a small high frequency signal to a large high frequency signal for transmission through a microwave antenna to another microwave antenna. As the required distance between the microwave antennas increases, more power is required at the base station to transmit. In this paper, we describe how to design a microwave power amplifier at 2.4 GHz starting from a MOSFET transistor chip to the actual board layout.

The transistor used here is the **Freescale Semiconductor** Transistor, part #MRF6S23140H. This part is designed for CDMA base station applications with frequencies from 2.3 to 2.4GHz. This transistor is characterized as follows at the quiescent operating point with targeted frequency of 2.4GHz. The load line and S matrix were determined through simulations. This resulted in unilateral operation of the transistor which implies a simpler matching network because there is no internal transistor feedback. Source and load matching networks are designed at 50 ohms with the corresponding S matrix. Stability was simulated and proven to be stable for the specified biasing range of the part. In addition, IP3 and 1 dB compression was graphed for the part.

Using these transistor characterizations, the completed microwave amplifier designs were simulated and the results are as follows. The theoretical amplifier gain is 18dB. The simulated gain before tuning is 14.3dB. The tuned amplifier gain, i.e. adjusting the matching network in real-time, is 17.0 dB. The 2 stage amplifier gain with tuned interfaced networks is 19.2 dB. The specification of the transistor at nominal is 15.2 dB with a minimum gain of 13 dB and a maximum gain of 17 dB. Our results prove that the matching networks were successfully matched, and that our layout design, will efficiently work at the 2.4 GHz specification.

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Introduction:

Microwave power amplifiers are used to boost a small high frequency signal to a large high frequency signal for transmission through a microwave antenna to another microwave antenna. As the required distance between the microwave antennas increases, more power is required at the base station to transmit. In this paper, we describe how to design a microwave power amplifier at 2.4GHz starting from a MOSFET transistor chip to the actual board layout.

The design flow for the power amplifier begins with the transistor selection, characterization, matching networks, stability, and dynamic range. Next, the power amplifier is tested with the above parameters, and then tuned for maximum performance. Lastly, a two stage power amplifier is tested and tuned for maximum performance.

Results from the power amplifier designs include gain and return loss. These results are compared with each other and with the actual performance of the transistor. The most efficient power amplifier design is then laid out for the final PCB. This PCB can then be manufactured with the corresponding components to complete the actual microwave power amplifier.

Design Flow:

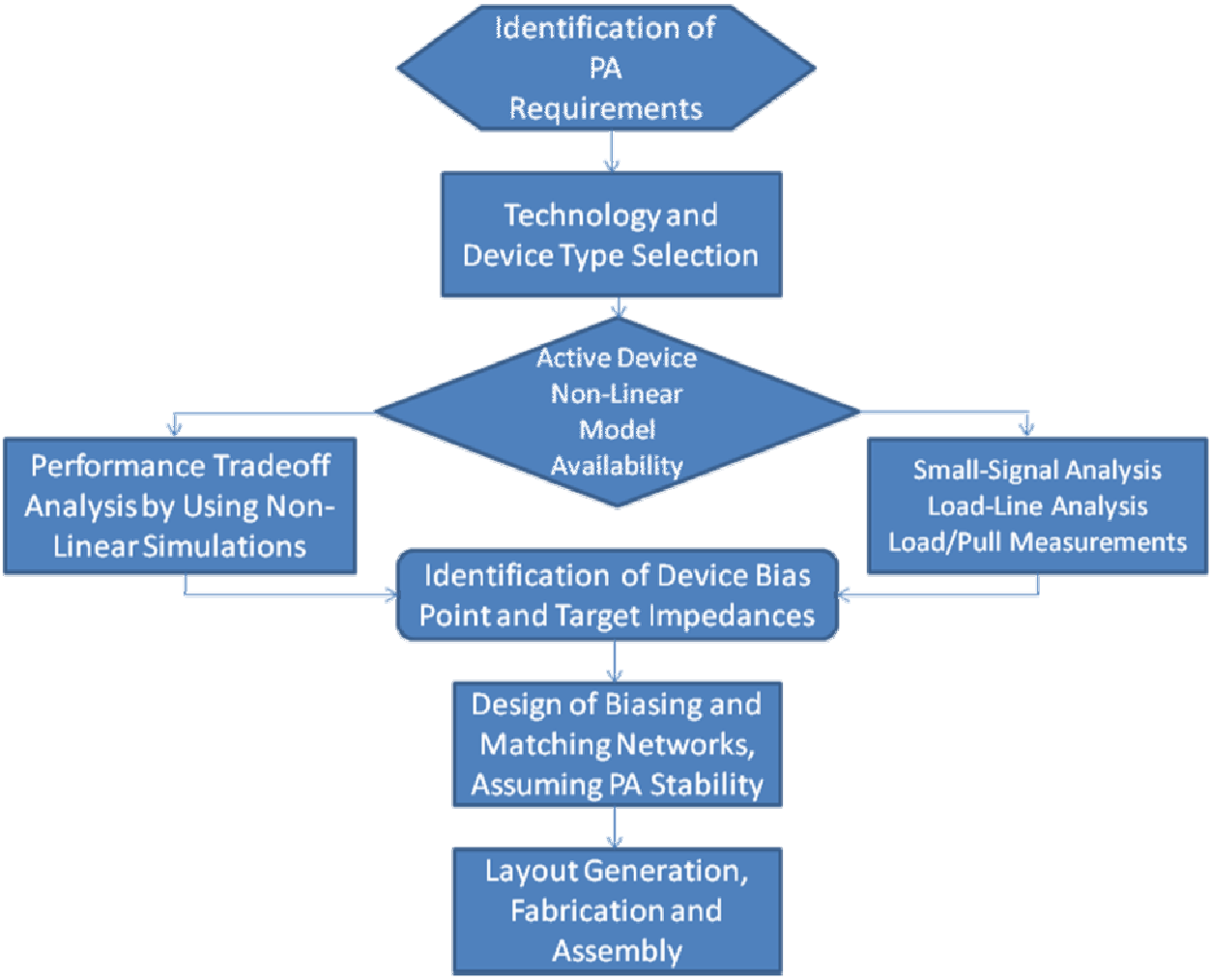

Figure 1. Design Flow [1].

The design flow as shown in Figure 1 is described below in an outline format as follows:

(1) **Identification of Power Amplifier Requirements:**

The power amplifier is a base station operating at 2.4GHz. In addition, the power amplifier must be buildable, i.e. the parts must exist to build it.

(2) **Technology and Device Type Selection:**

The device type is a MOSFET by Freescale Semiconductor, part #MRF6S23140H. The MOSFET device was chosen because it will be easier to do source and load matching networks especially if the device is determined to be unilateral.

(3) **Active Device Non-Linear Model Availability:**

This is available.

(4a) **Performance Tradeoff Analysis by using Non-Linear Simulations**:

This is available.

(4b) **Small Signal Analysis, Load-Line Analysis, Load/Pull Measurements:**

This is available.

(5) **Identification of Device Bias Point and Target Impedances:**

The transistor's quiescent point is in the data sheet, but the S parameters are unavailable and must be determined through simulations.

(6) **Design of Biasing and Matching Networks Assuming Power Amplifier Stability:**

The design of biasing and matching networks are first determined theoretically and then simulated. The biasing versus stability is later simulated.

(7) **Layout Generation, Fabrication and Assembly:**

The most efficient design is laid out for fabrication.

Characterization:

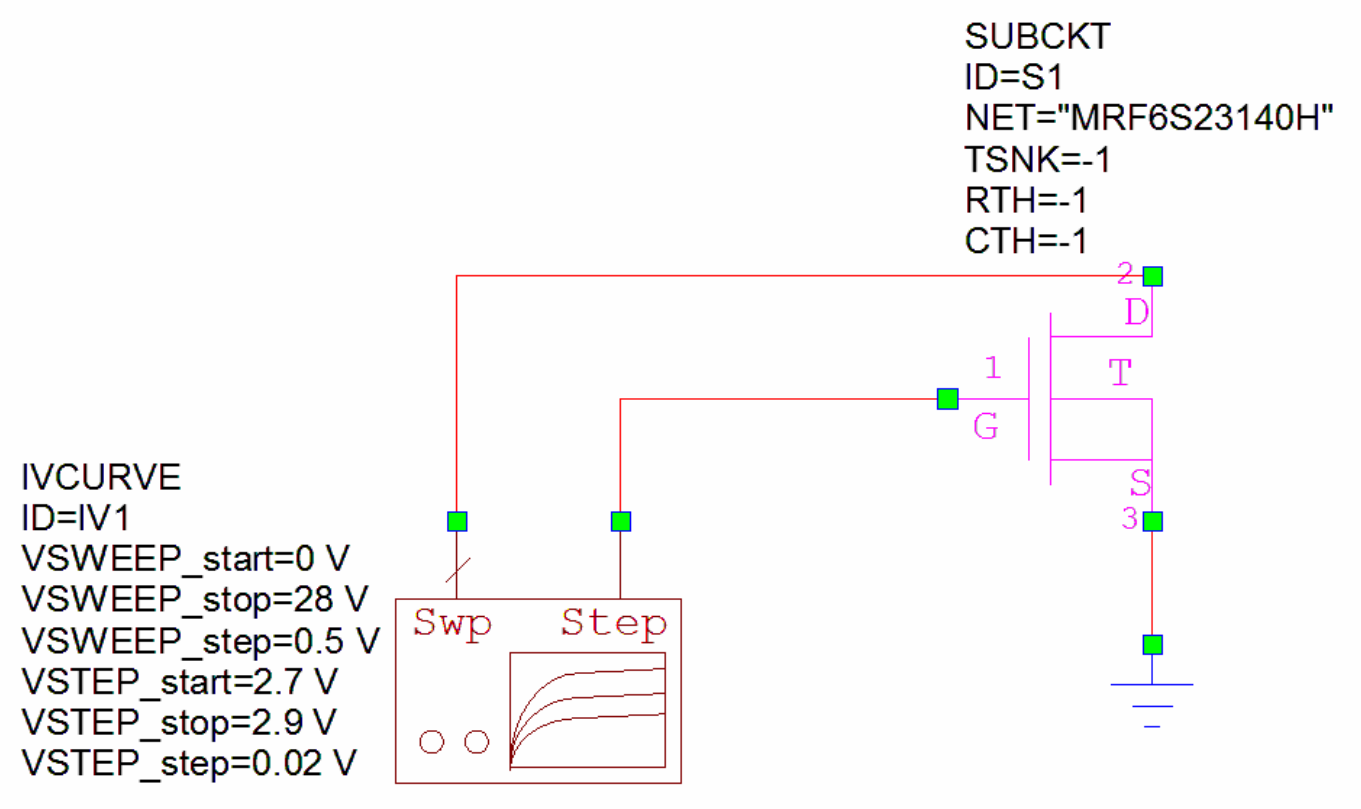

Figure 2. Curve Tracer Setup.

Transistor characterization is performed by a curve tracer that steps the voltage from gate to source and sweeps the voltage from drain to source as shown in Figure 2. The corresponding IV curve is plotted in Figure 3. A summary of the data sheet is shown below with the complete data sheet in Appendix I:

Freescale Semiconductor Part #MRF6S23140H Rev. 2, 12/2008
2300-2400 MHz, 28 W AVG., 28 V
Class AB and Class C applications
VDD = 28 Volts, IDQ = 1300 mA, VGS = 2.8 Volts
Pout = 28 Watts Avg., f = 2390 MHz,
Channel Bandwidth = 3.84 MHz,
Power Gain — 15.2 dB

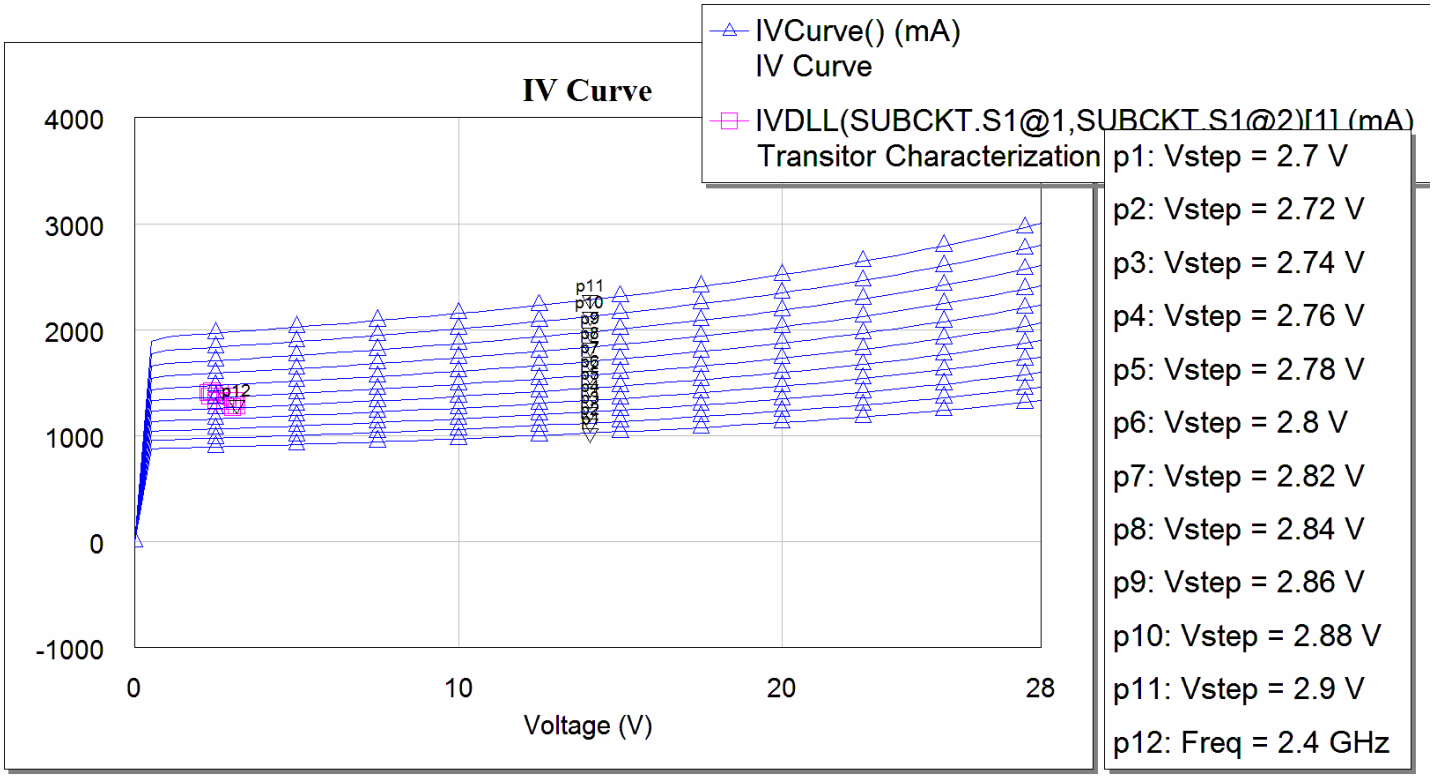

Figure 3. Transistor's IV Curve: The magenta line in Figure 3 is the load line at the quiescent operating point of 1300 mA, Vgs = 2.7 V and Vdd = 28 V.

Two Port Scattering Matrix:

In order to determine the scattering matrix of our **Freescale** transistor we performed a frequency sweep of the S Parameters. This sweep is shown in Figure 4. This sweep was done with our transistor biased at I_D=1.33A, V_{GS}=2.7V, and V_{DD}=28V. These biasing conditions are all very close to the quiescent conditions shown in the transistors data sheet. We then extracted the S Parameters of the transistor at 2.4GHz.

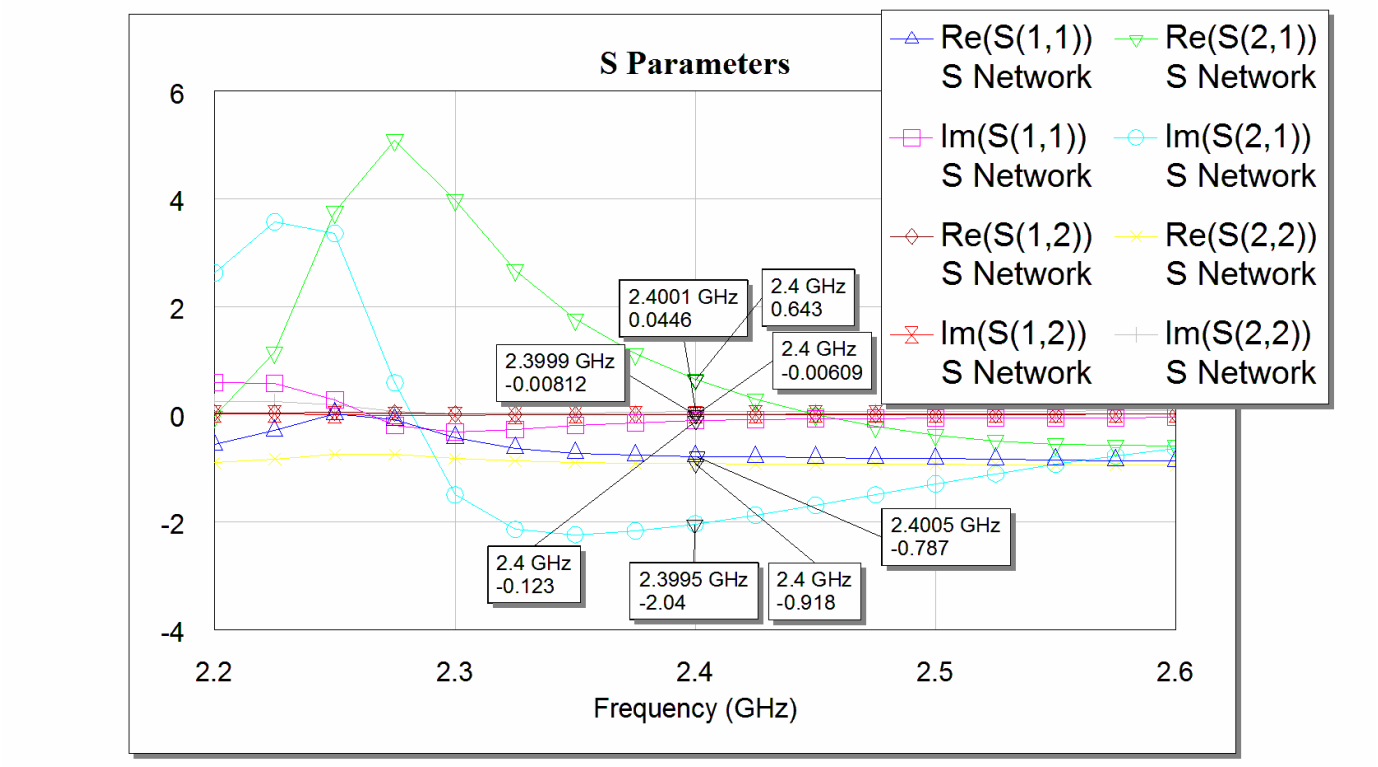

Figure 4. S Parameters of transistor from frequency sweep of 2.2GHz to 2.6GHz.

The 2.4GHz S parameters are shown below in the following scattering matrix:

$$[S] = \begin{bmatrix} .744\angle -170^\circ & .01\angle -143^\circ \\ 2.12\angle -72.5^\circ & .917\angle 177^\circ \end{bmatrix}$$

It should be noted that S_{11} and S_{22} should both have magnitudes less than one to maintain stability. Also, since the transistor gain is the square of the magnitude of S_{21} this value should be greater than one to have gain greater than unity. This is explained in greater detail in the stability section and the conjugate matching section of this report.

Unilateral Condition:

A transistor is unilateral if S_{12} is zero or very near zero when compared to the other S parameters of its scattering matrix [3]. From the S matrix that we determined for the **Freescale** transistor, the S_{12} term is very small and can be set to 0 to simplify our amplifier calculations. With this assumption, there will be no internal feedback. This means the input resistance will be independent of the load resistance, and the output resistance will be independent of the source resistance. This will make designing the source and load matching networks easier. For example, the output matching network would see R_{ds} looking into the output of the transistor, and if the manufacturer of the transistor would make R_{ds} = 50 ohms, then a matching network would be minimal.

Stability:

A successful amplifier design requires a number of characteristics to be met including voltage gain, power gain and linearity, but perhaps the most critical aspect of any amplifier is stability. Even if a design produces excellent gain and linearity, if it is unstable it is essentially unusable. For this reason it was vital for us to consider stability through every step of the design process. Stability of an amplifier is its immunity to causing spurious oscillations. In the case of high-frequency amplifiers, there are two types of stability defined: conditional stability and unconditional stability. If an amplifier is conditionally stable, it is shown to be stable with both ports properly terminated (that is, with the intended source and load impedances). A much better result is unconditional stability, which shows

that an amplifier is stable regardless of input and output impedances. In our analysis we sought to determine unconditional stability for this amplifier design. If the transistor is not unilateral the following conditions must be met to determine unconditional stability:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \qquad \text{AND} \qquad |\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \qquad [3]$$

To facilitate the determination of this key factor, we needed to first establish that our circuit was unilateral; that is, signal flows only in the forward direction or, equivalently, S_{12} (transmission from port 2 to port 1) equals zero. If the unilateral condition is met, calculations required for unconditional stability determination simplify greatly, requiring only two conditions. These are:

(1) $|S_{11}| < 1$ and (2) $|S_{22}| < 1$

Using AWR Microwave Office, we characterized our circuit's scattering parameters through simulation and were able to show that the unilateral condition was met.

To determine the stability of the circuit we needed to examine the magnitude of input and output reflection coefficients as various parameters of the circuit were varied to find if any condition existed which would cause either of these magnitudes to exceed unity. We used the tuner tool in Microwave Office to facilitate this determination by varying the quiescent bias point and observing how the scattering parameters changed as a result. To clearly see the magnitudes of the reflection coefficients, we plotted all four S-parameters on a polar chart to show magnitude an phase. This is shown in figure 14. As we varied the quiescent point of the transistor we watched how S_{11} and S_{22}

moved on the chart, paying close attention to whether these parameters ever moved outside of the unit circle. Fortunately, regardless of how far we moved the bias point from our nominal value, we were unable to force S_{11} or S_{22} greater than unity, showing that our circuit was unconditionally stable.

Conjugate Matching Networks:

Conjugate matching is used to transfer the maximum amount of power from the source to the transistor and from the transistor to the load [3]. Maximum power transfer from the source to the load occurs when the real part of the source matching network equals the real part of the input impedance of the transistor and when the imaginary part of the matching network is the conjugate of the imaginary part of the input impedance of the transistor [3]. This can be written much more succinctly in mathematical form as:

$$\Gamma_S = \Gamma_{in}^* = S_{11}^*$$

After plugging in the complex conjugate of S_{11} we determined the reflection coefficient of the source matching network seen from the transistor as being the following:

$$\Gamma_S = .744\angle 170^\circ$$

It should be noted that taking the complex conjugate of a reflection coefficient results in the complex conjugate of the corresponding impedance being taken. Thus either reflection coefficient or impedance can be used for conjugate matching. Since we already have the reflection coefficients of our transistor from its scattering matrix it is simpler to deal with reflection coefficients.

The same argument was used to determine the output matching networks required reflection coefficient:

$$\Gamma_L = \Gamma_{out}^* = S_{22}^*$$

$$\Gamma_L = .917\angle -177^\circ$$

Figure 5, below, shows the basic block diagram that we used to design our microwave amplifier. Knowing the S parameters of our transistor was the main key to being able to design our microwave amplifier circuit.

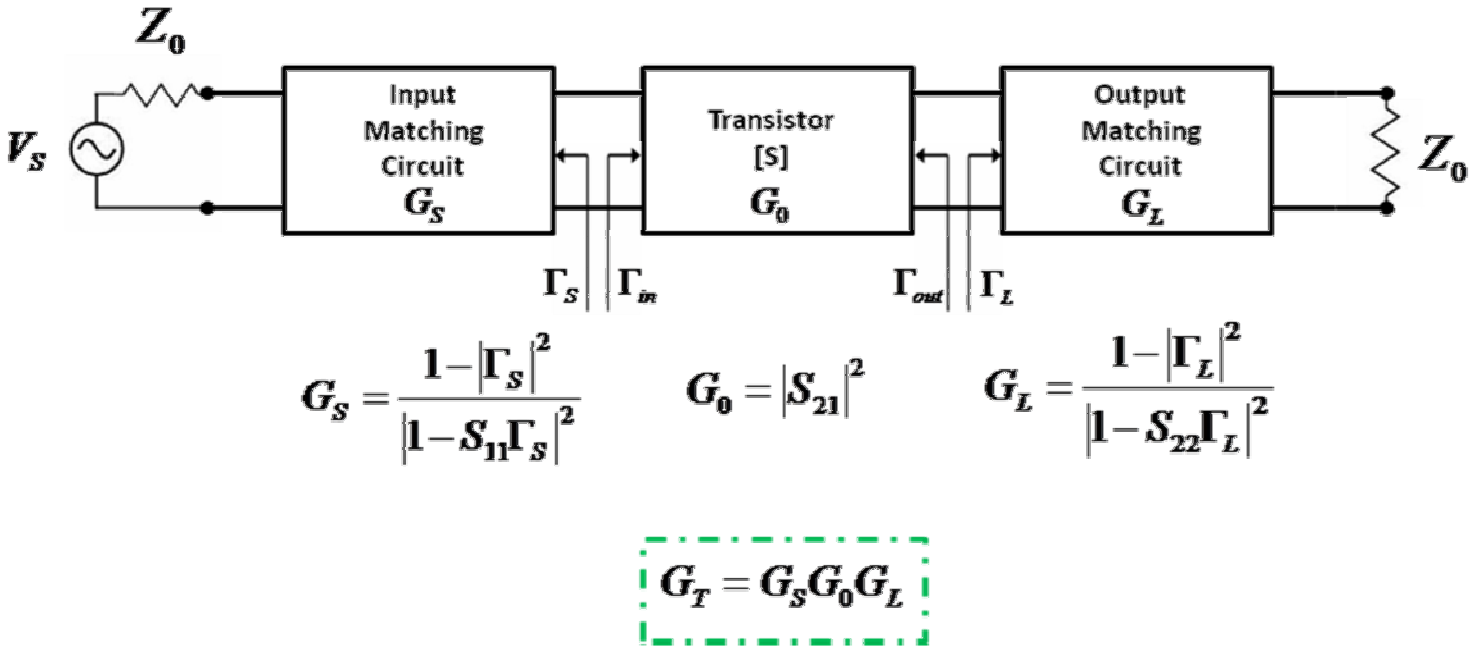

Figure 5. Microwave amplifier block diagram showing the source matching network, transistor, and output matching network with the gain of each stage and total transducer gain noted [3].

From figure 5 the gains of each stage can be seen. G_S is the input matching network gain, G_0 is the transistor gain, and G_L is the output matching network gain. These three gains combined are the total gain of the amplifier circuit known as the transducer gain, G_T. Smith charts were used to determine the input and output matching networks required for conjugate matching. We used an open shunt stub followed by a transmission line to take us from the port impedance of 50Ω to the required input matching and output matching network impedances. These impedances exist at the same point as the input matching and output matching reflection coefficients respectively.

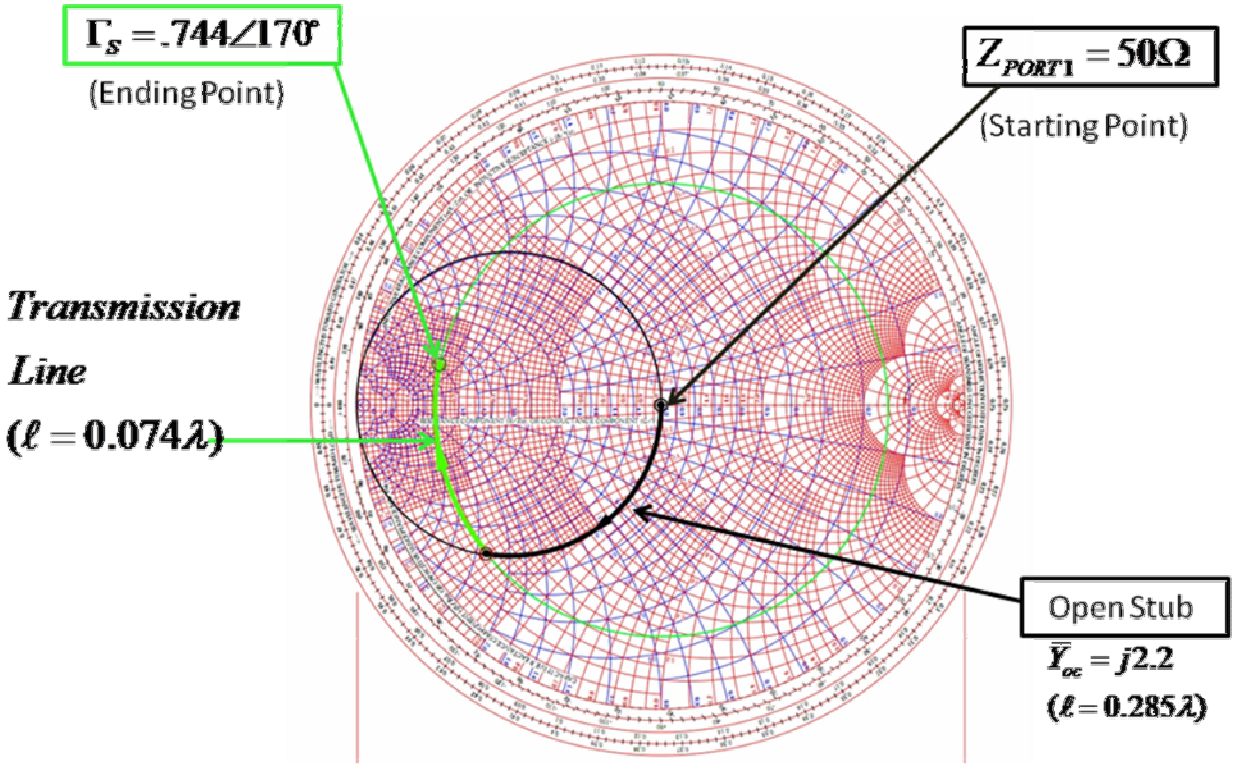

Figure 6. Smith chart showing source matching method, note that the shunt open stub and transmission line lengths of the matching network are shown.

Figure 6 shows our path from port 1, the source, to our required source matching network impedance that exists at the same point at the input matching network reflection coefficient. We first followed the constant conductance circle using an open stub of length 0.285λ to where it intersects with the VSWR circle of our input matching network impedance. We then followed a transmission line of length 0.074λ to our final destination denoted as Γ_S.

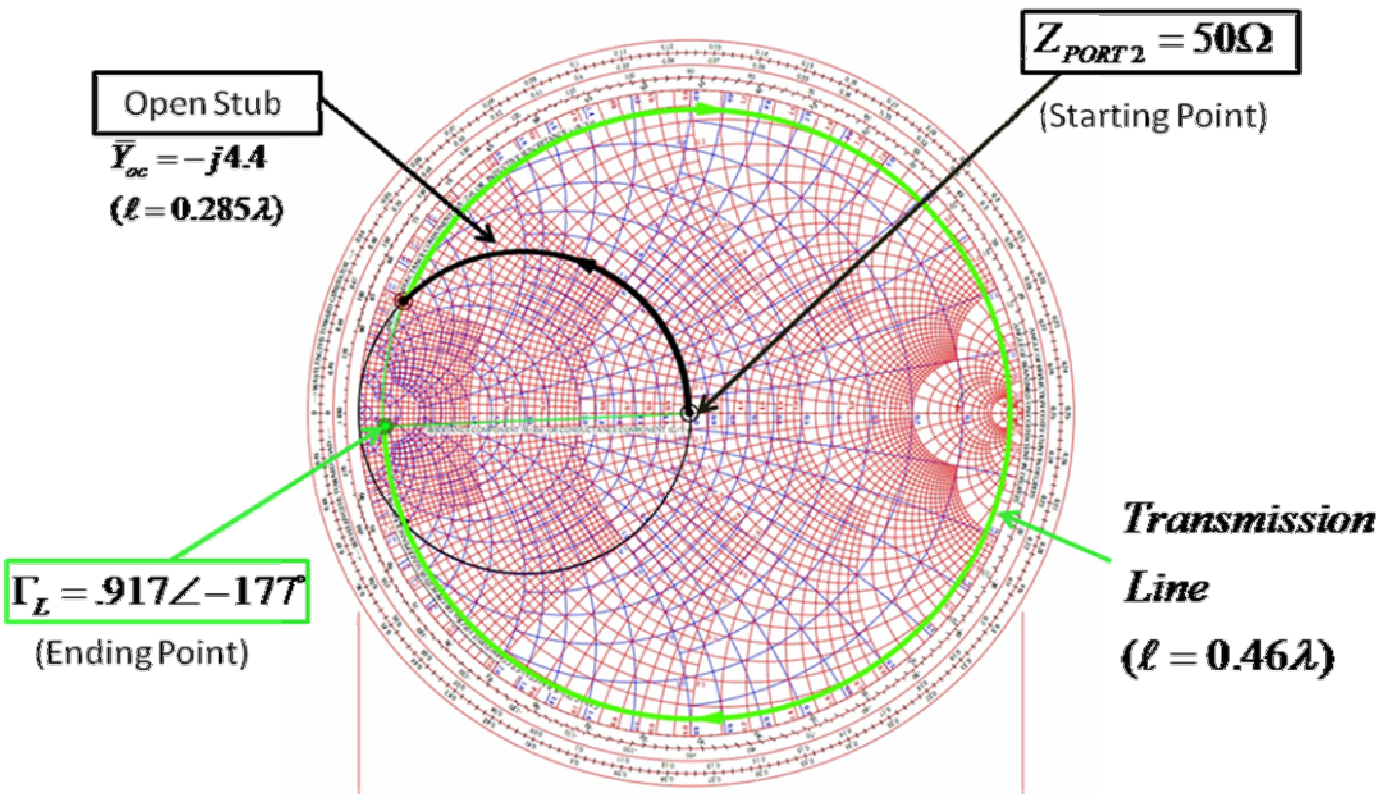

Figure 7. Smith chart showing conjugate matching method at the load similar to the source matching method.

Our path from the output port, port 2, to our required output matching impedance is shown in figure 7. Once again we started at 50Ω, which is our load impedance. We then followed an open shunt stub of length 0.285λ along a constant conductance circle until we hit the intersection point of this circle and the VSWR circle on which our required output matching load impedance exists. After hitting this VSWR circle we then traveled on a transmission line of length 0.46λ to land at our required output matching network impedance.

Power Amplifier Design:

After we determined what our input matching and output matching network stub and transmission line lengths were we were ready to simulate our amplifier using **AWR**.

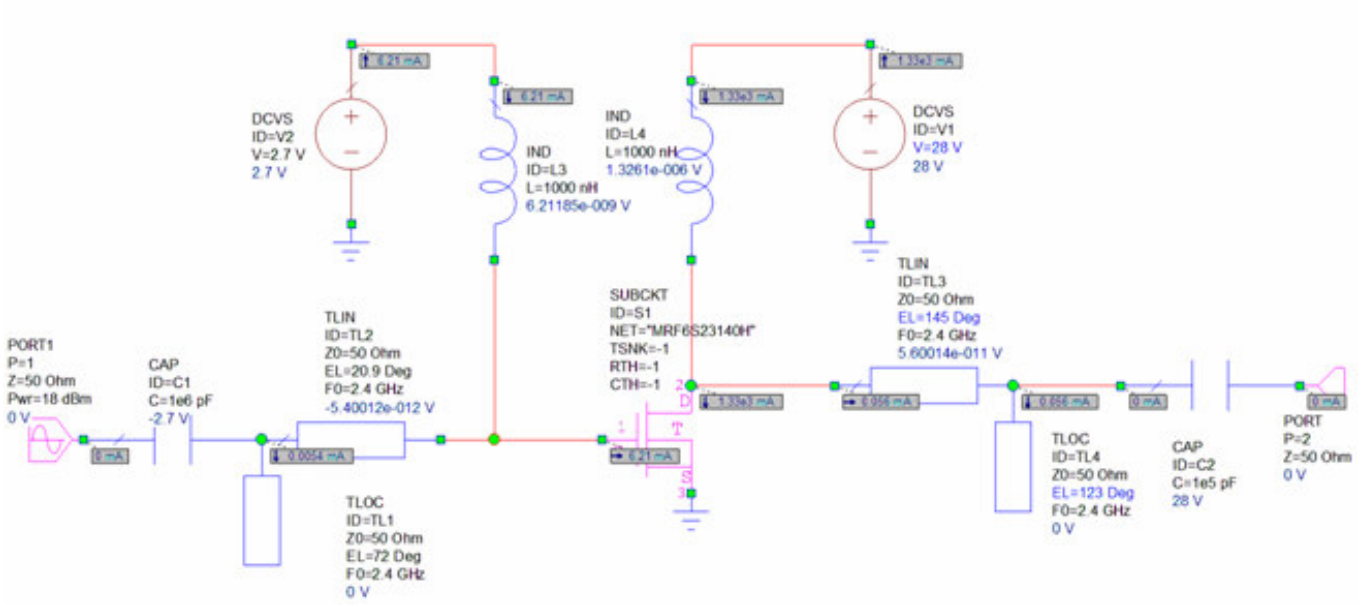

Figure 8. Power Amplifier Circuit with source and load matching networks, and biasing circuit.

Biasing Circuit:

The biasing circuit of figure 8 has been designed with two voltage sources versus having one V_{dd} source because it was easier to vary the two individual voltage sources independently. After the voltage source is an inductor. The inductor will act like an open at high frequencies. This will prevent the high frequency signal from going down that circuit path. Note, there are no resistors in the biasing network since they will only introduce losses in the network. The last elements are the capacitors at either end. They will prevent the biasing voltage from going down the signal path because they will act like opens at DC. The values chosen for the voltage supplies are 2.7V at the gate and 28V at the drain. With this combination, the quiescent operating point is achieved with a current of I_{ds} = 1.3A. Note that it was found that the source is internally connected to ground, so we were unable to place any components there other than ground.

Amplifier Gain:

Based upon the gain equations shown in figure 5 a theoretical amplifier gain was determined as follows:

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} = 2.24 = 3.50dB$$

$$G_0 = |S_{21}|^2 = 4.49 = 6.52dB$$

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = 6.28 = 7.98dB$$

$$G_{T,dB} = G_{S,dB} + G_{0,dB} + G_{L,dB} = 18dB$$

This theoretical gain of 18dB is the best gain that we could expect under perfect matching conditions.

The gain and return loss results of our **AWR** simulation of the circuit shown in figure 8 are shown in figure 9.

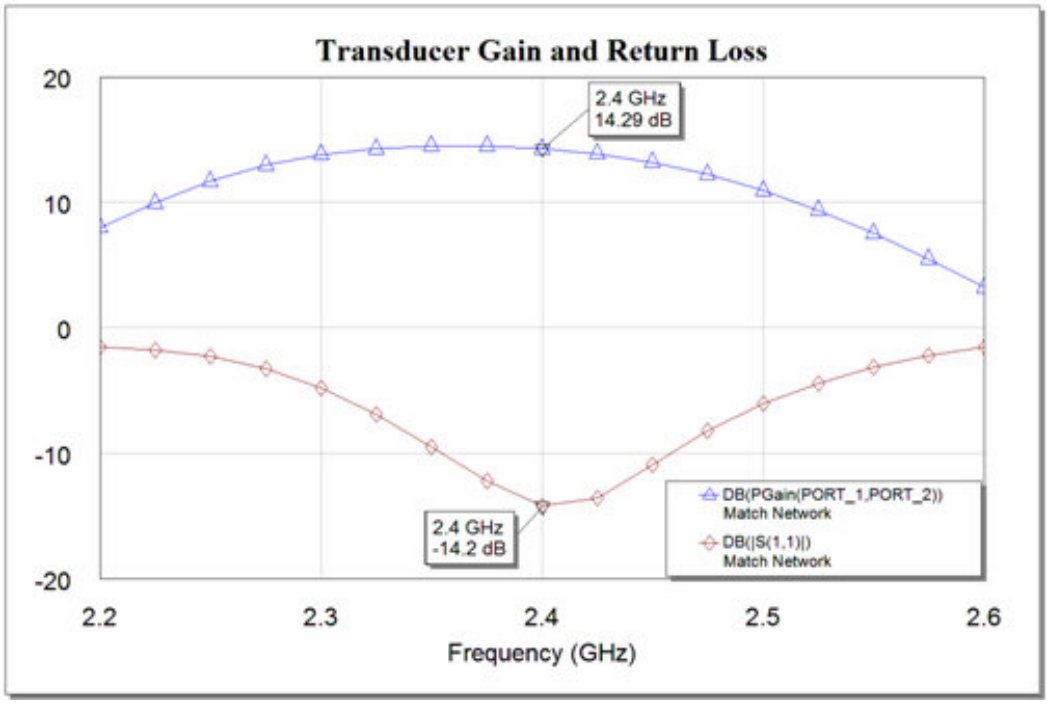

Figure 9. Transducer gain and return loss of amplifier circuit plotted on a power gain in dB vs frequency set of axes. The Blue line is gain, and the pink line is the negative of our return loss.

From the plot of figure 9 it can be seen that the gain of our amplifier circuit is 14.29dB at 2.4Ghz and the negative of our return loss is -14.2dB. This gain is below our theoretical maximum, which is expected, but it still lies between the expected range of the data sheet of 13 to 17dB. It should also be noted that our return loss maximizes at our operating frequency of 2.4GHz, this means that we have maximum transmission from source to transistor at our operating frequency.

After seeing what our results were from the Smith chart predicted matching networks we decided to tune the transmission line and stub lengths of our matching networks using the

tuner tool of **AWR**. After tuning these lengths for maximum gain we arrived at the plot shown in figure 10.

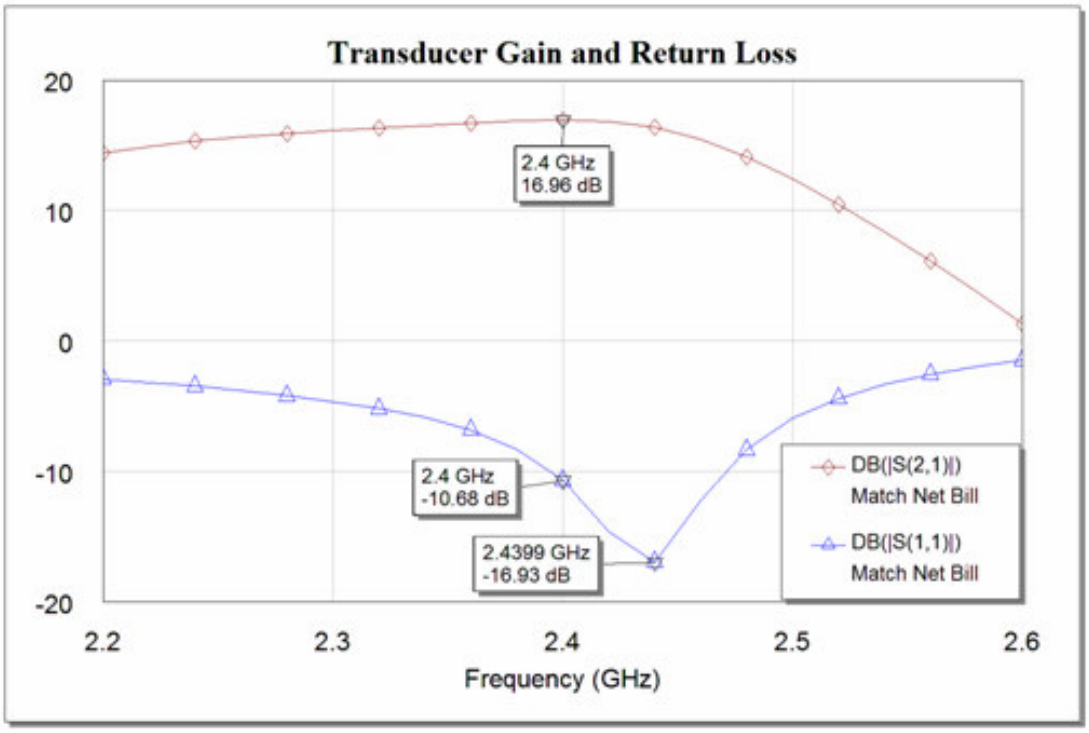

Figure 10. Tuned transducer gain and return loss. Here the pink line is our gain and the blue line is the negative or our return loss.

It can be seen from figure 10 that tuning our matching network gave us an additional gain of 2.7dB, but our return loss decreased by 3.6dB. This amplifier setup is thus less efficient because input energy is lost, but it does have a higher gain.

Dynamic Range:

The dynamic range is the linear range of the graph in Figure 11, a dB plot of output power versus input power, where the minimum is the noise floor, approximately -60 dB (Note, noise floor data was not available for this part and a rough estimate of the noise floor is assumed based on previous parts of this type.), to a maximum value of 42.5 dB, i.e. the 1 dB compression point from Figure 12.

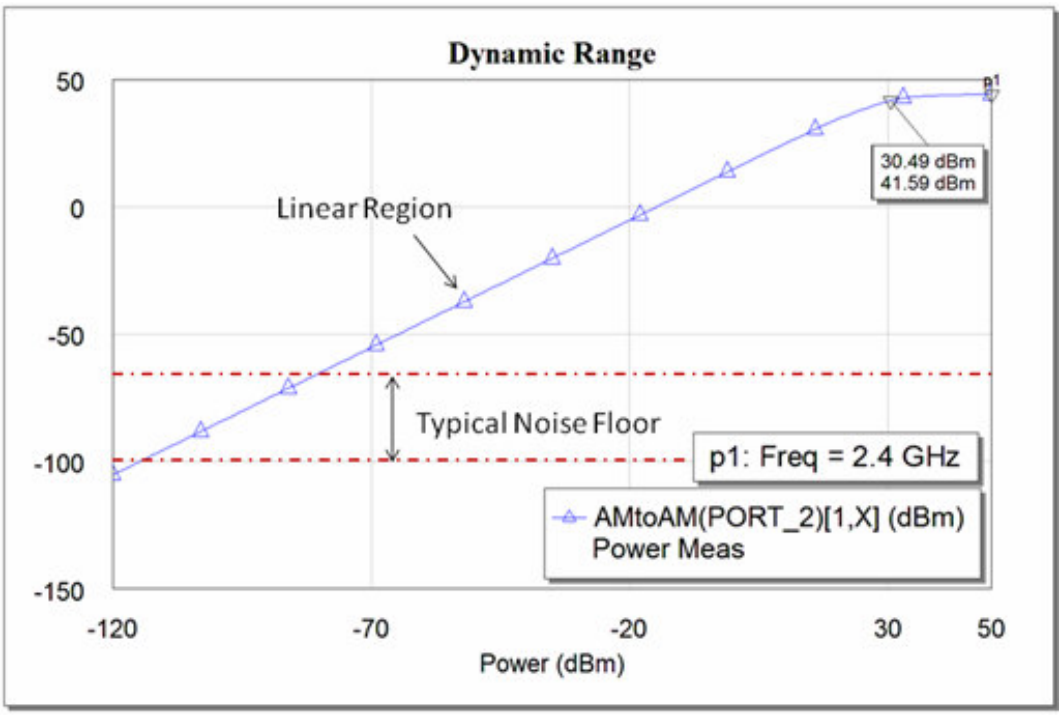

Figure 11. Dynamic range of our amplifier.

The 1 dB compression point in Figure 12 is defined at the upper range of the graph where the linear part of the graph is extended past the nonlinear part of the graph where the vertical distance between the two graphs is 1 dB. This value is the maximum possible value where the relationship is still linear.

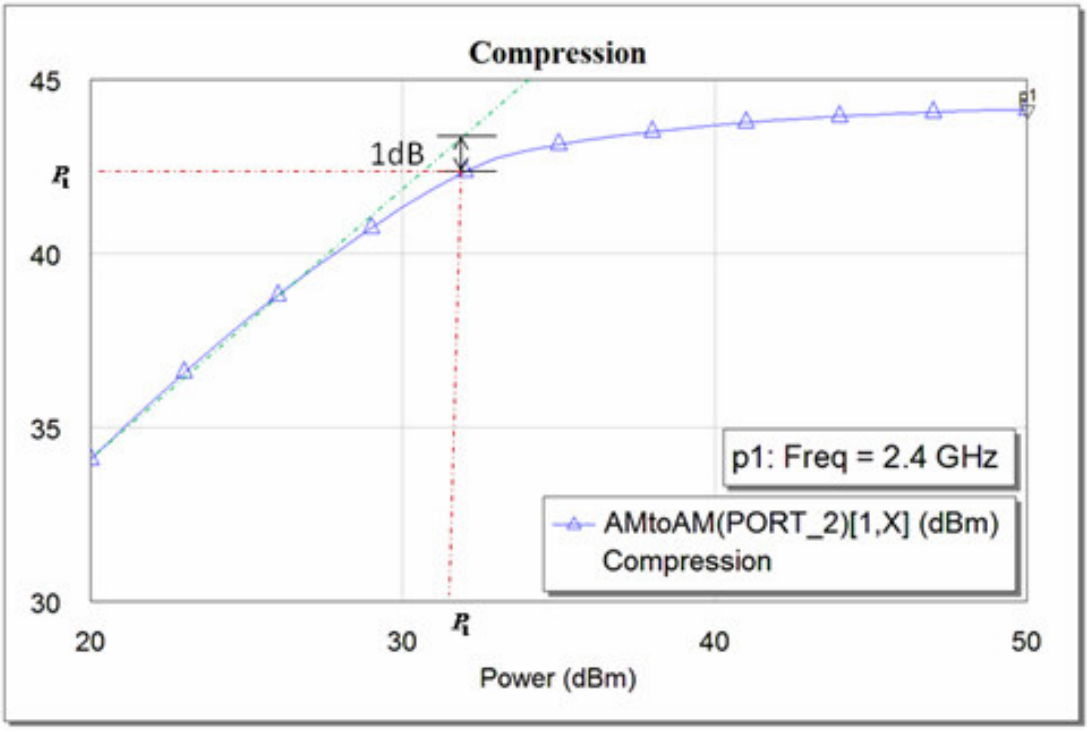

Figure 12. 1 dB compression point of our amplifier.

This upper range still needs to be interpreted in terms of its intercept point. The concept of intercept point means that higher-order nonlinear terms are negligible. However, the weakly nonlinear assumption does not hold for the upper end of the input power range. These results in the simulated data deviating from the ideal slope of three assuming the third order intercept point.

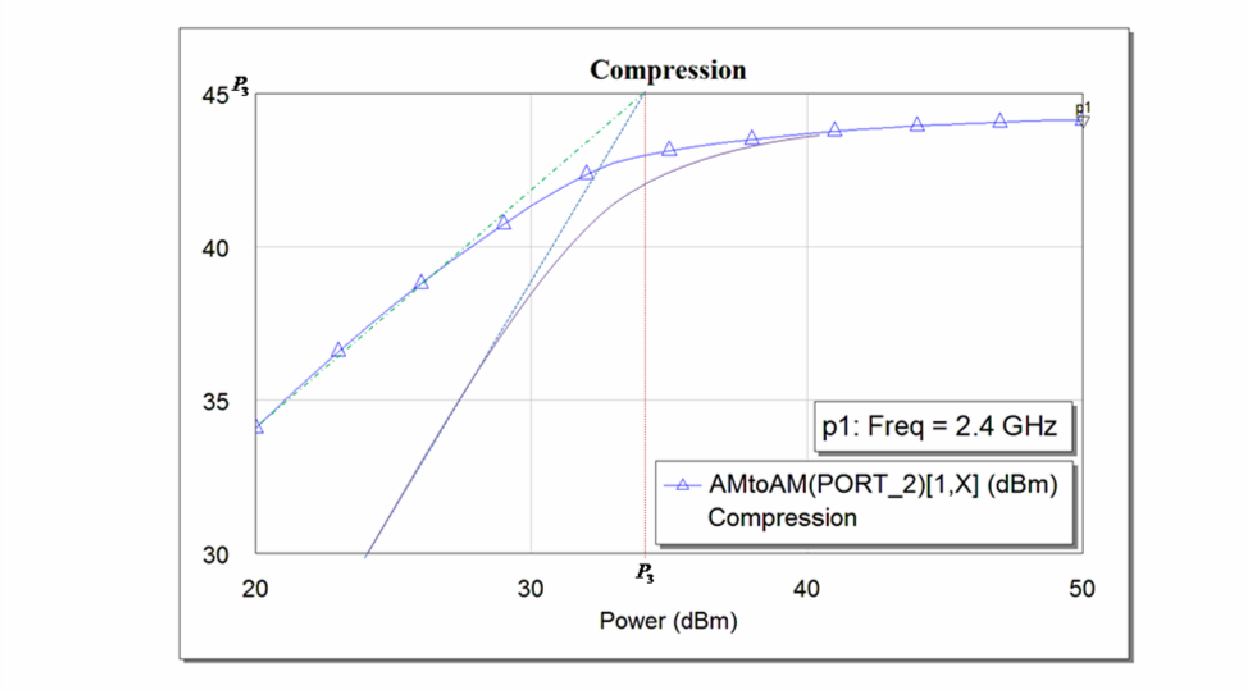

Figure 13. IP3: Third Order Intercept Point

The third order intercept point is determined as follows and is shown in Figure 13. The intercept point is obtained graphically by plotting the output power (dBm) versus the input power (dBm). The linear amplified signal has a slope of one, and the third order nonlinear product will have a slope of 3 dBm. Both curves are extended linearly until they intersect. This is defined as the third order intercept point. This value is 45 dBm.

In determining the upper range, as a rule of thumb, the 1 dB compression point should be 10 dBm below the IP3 intercept. In this case, IP3 is 45 dBm, and 1 dB compression is as 42.5 dBm. Hence, using the 1 dB compression would introduce nonlinear terms in the upper ranges, i.e. above 35 dBm. Therefore, the dynamic range will be computed using the rule of thumb and is 95 dBm. This process can be repeated for high order intercept points like IP5. Note, IP3 is an approximate curve.

Biasing Versus Stability:

In an attempt to make our amplifier circuit unstable we turned the drain current up to 3.9A. This current is much higher than the recommended biasing current and would probably result in a thermal meltdown of the part. But, as theoretical stability is concerned the system remained stable.

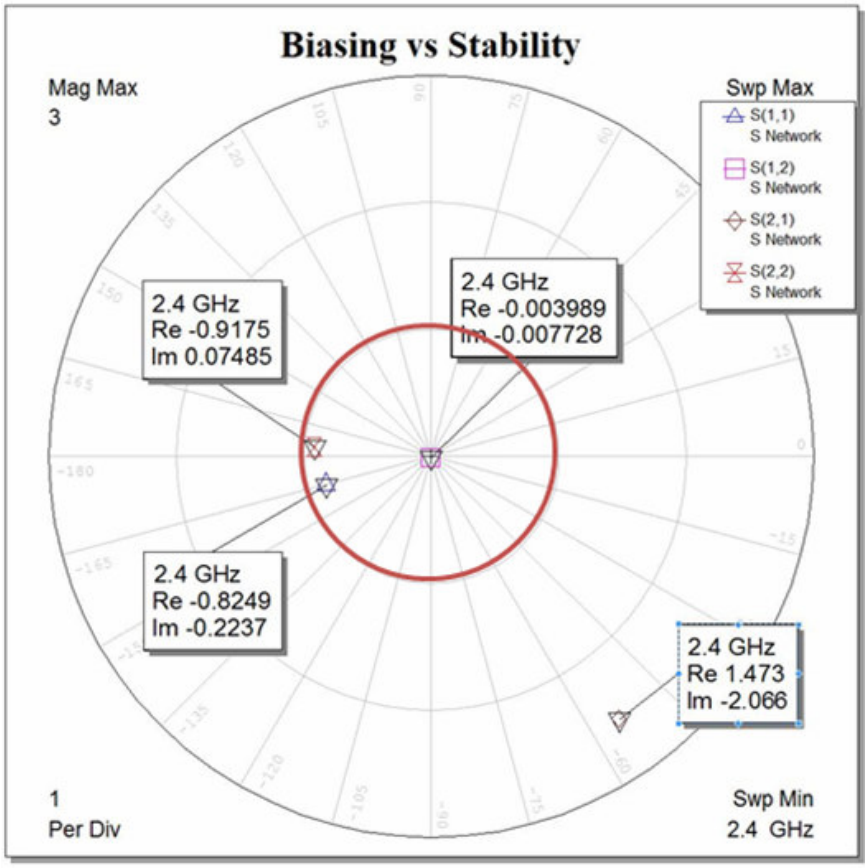

Figure 14. Unit circle, the red circle, showing amplifier stability: here we have turned the bias current way up and S_{11} and S_{22} have remained inside the unit circle showing that the system is still stable.

Figure 14 shows our S parameters at this new bias current of 3.9A. It is important to note that S_{11} and S_{22} still have magnitudes less than one, and S_{12} is still negligible. Also, the magnitude of S_{21} has increased, which is expected.

PCB Layout:

After the circuit had been designed we wanted to provide a way for it to be assembled, tested, and used in the future. To make this possible, we designed a printed circuit board (PCB) which included all of the components and transmission lines (microstrips) that we selected in our design. The completed PCB design is shown in figure 15. Comparing the board layout to the circuit design, it is easy to see how each of the components is arranged by tracing from the input port to the output port (which are labeled on the board). C1 and C2 are the DC blocking capacitors for input and output, respectively. L1 and L2 are the DC bias and drain pull-up inductors, C3 and C4 are DC filtering capacitors for the main and bias voltage supplies and of course Q1 is the transistor.

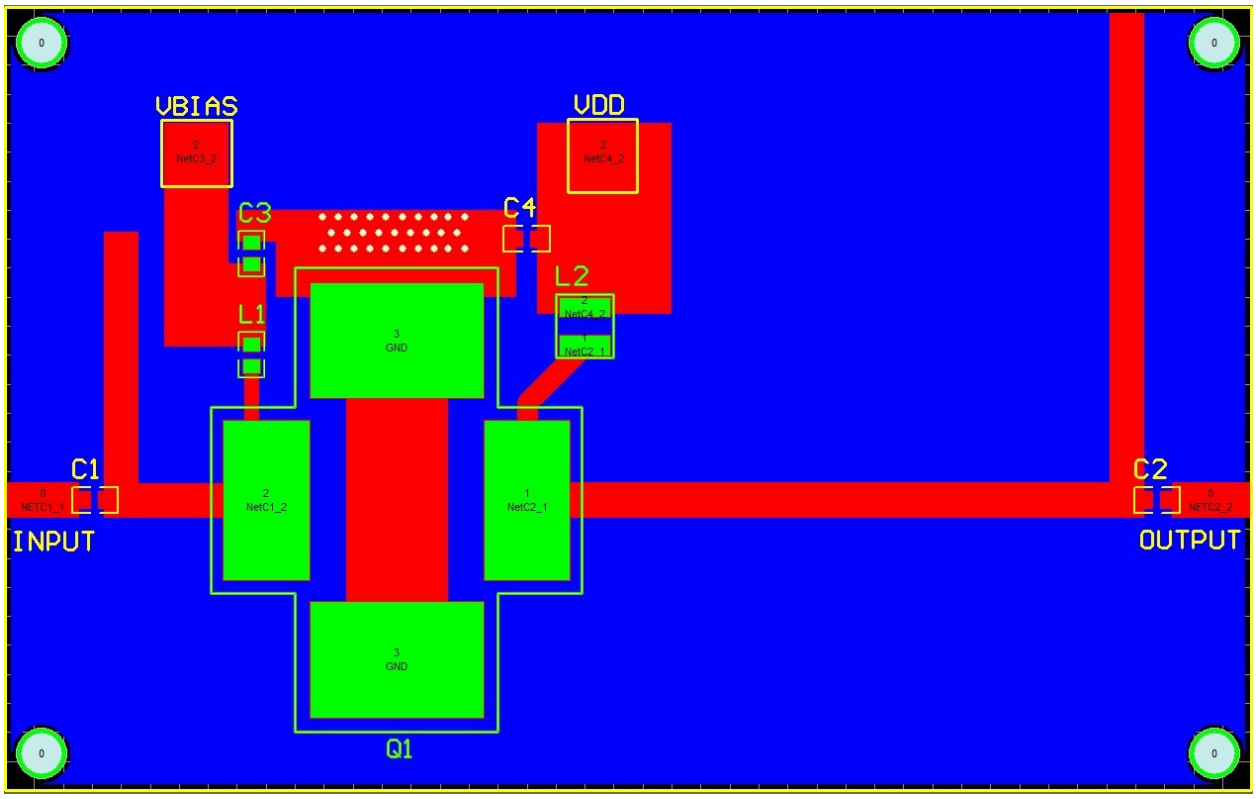

Figure 15. PCB Layout of single stage amplifier.

The board was designed assuming FR4 substrate material 68mil thick with 1oz. copper on both sides. The necessary width for the 50Ω traces was calculated using an online applet designed for just this use. The board thickness, permittivity, copper weight and desired impedance were entered in to the calculator applet which provided the appropriate trace width. Using this width along with the lengths determined for the transmission lines of the matching networks, the board was easily laid-out using the **Altium Designer** electronic design software suite. In figure 15, the red traces are all on the top layer and the blue background is a full ground-plane fill on the bottom layer. The source of the transistor is connected to the ground plane by an array of via holes to provide a low impedance connection.

Two Stage Power Amplifier Design:

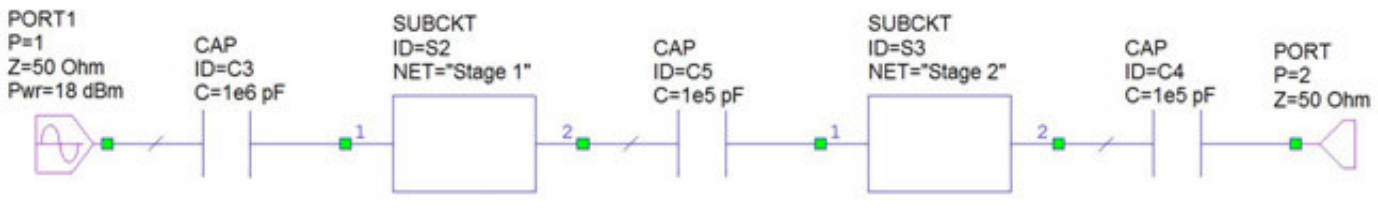

Figure 16. Two Stage Power Amplifier with stages one and two being sub-circuits.

Why use a two stage amplifier design? Because a single stage amplifier does not have the required gain. So does a two stage amplifier design produce a 14dB + 14dB gain. No, the second

transistor would saturate and generate lots of noise. How do you design a multiple stage amplifier? In designing a multiple stage amplifier, it is important to limit the noise from being amplified. It doing so, the first stage would have the maximum gain and every succeeding stage would be at least half the previous stage with the last stage having only a gain of 2. Having a large number of amplifiers in series has diminishing returns. The number of amplifiers in series usually does not exceed 4, and the fourth one is usually a buffer or a 2x multiplier. Using our previous designed microwave power amplifier, a two stage amplifier is designed as shown in Figure 16, and the simulation results are presented.

From Figure 16, capacitors are present so the biasing network does not extend into other circuitry. The first stage is the same as previously discussed. The second stage is designed with considerably less gain for reasons previously discussed.

In each stage there is a matching network associated with the source and load. Note, because of the unilateral property, the source and load matching networks will not need any tweaking. However, interfacing stage 1 to stage 2, the impedance matching is at 50 ohms and required two matched networks. Another option is to use one matching network where the load is the second stage which would not be 50 ohms. Again, this would be okay because of the unilateral property. The advantage of using one match load is obviously the losses associated with an additional matched network. Anyways, beginning with the two matched networks, the results were poor. That is, at 2.4 GHz the bandwidth was narrow and the gain was not much more. Using the tuning tool on both the networks, the results could be tuned.

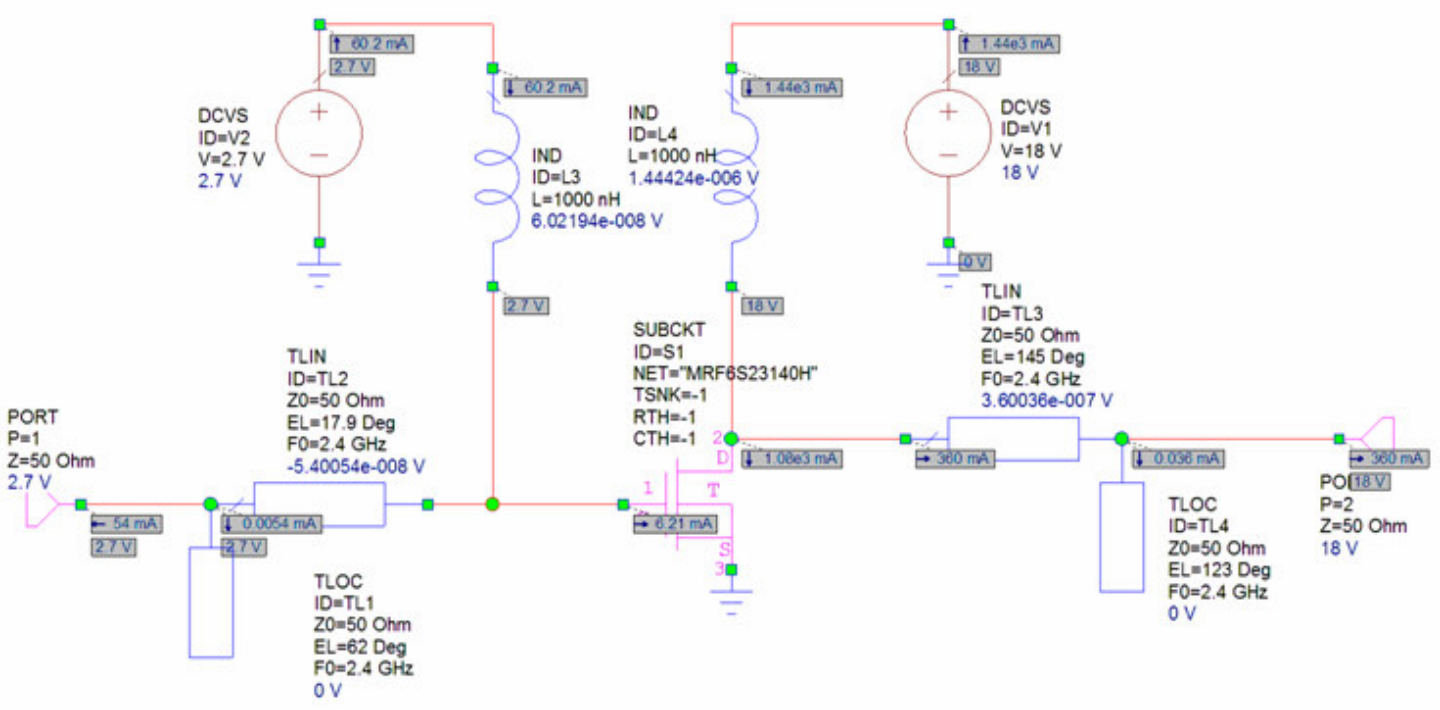

Figure 17. Second stage amplifier, sub-circuit "stage 2" of figure16.

The second stage is designed to produce considerably less gain than the first stage. The goal is to achieve a gain around 20 dB so the drain voltage supply was changed to 18 V and the resulting I_{ds} is 1.08 A. With this change, the S parameters will change, but we will still be operating at 2.4 GHz. The interface matched networks were tuned, and the results of this are presented next.

Two Stage Gain:

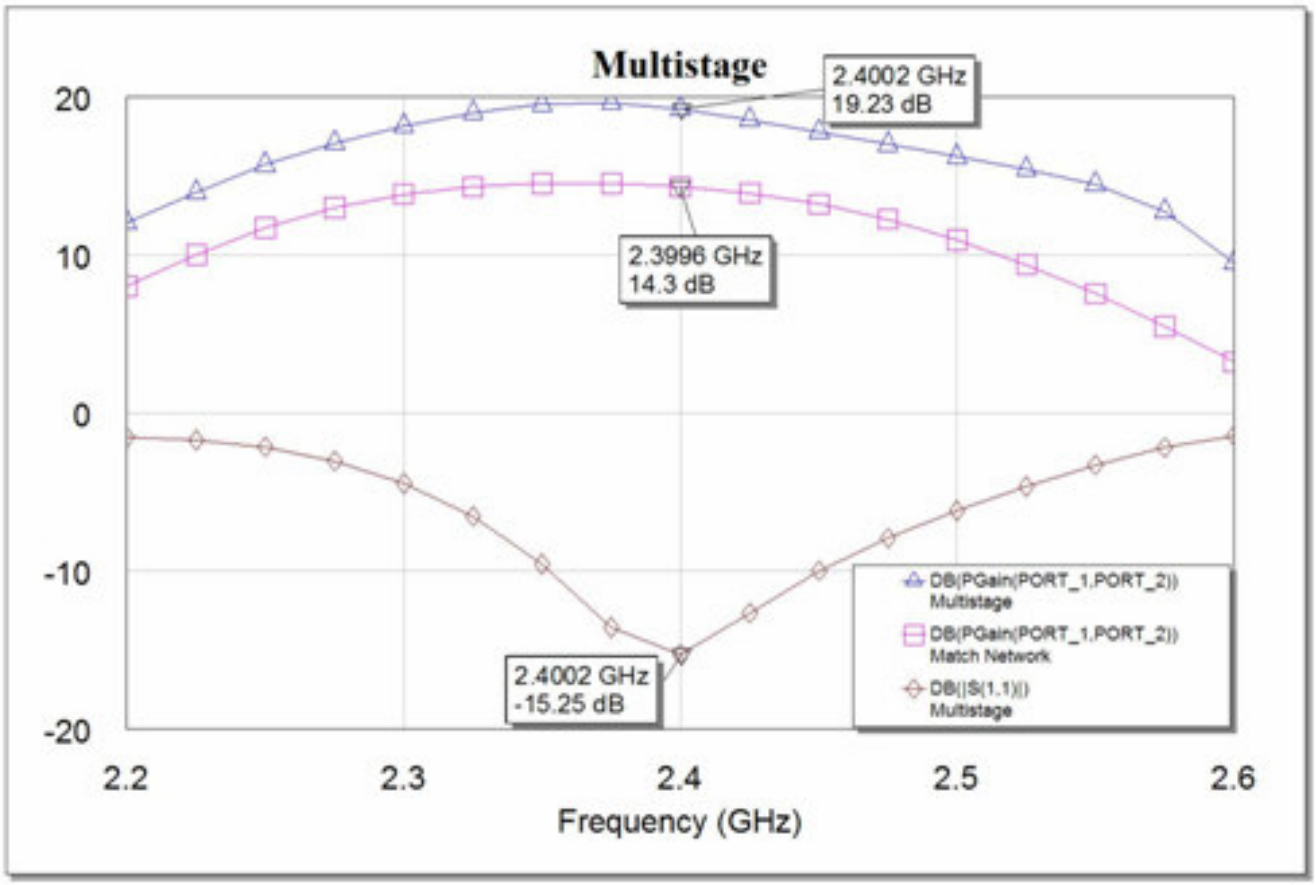

Figure 18. Two stage amplifier gain compared to single stage amplifier gain. The blue line is the two stage amplifier gain, and the pink line is the single stage amplifier gain.

The tuned two stage amplifier gain and return loss are excellent as shown in Figure 18. The pink curve is the theoretical gain from the single stage amplifier, i.e. see previous results. This two stage amplifier gain is shifted up and parallel with the single stage and the return loss peaks at 2.4GHz like the single stage amplifier.

Two Stage Dynamic Range:

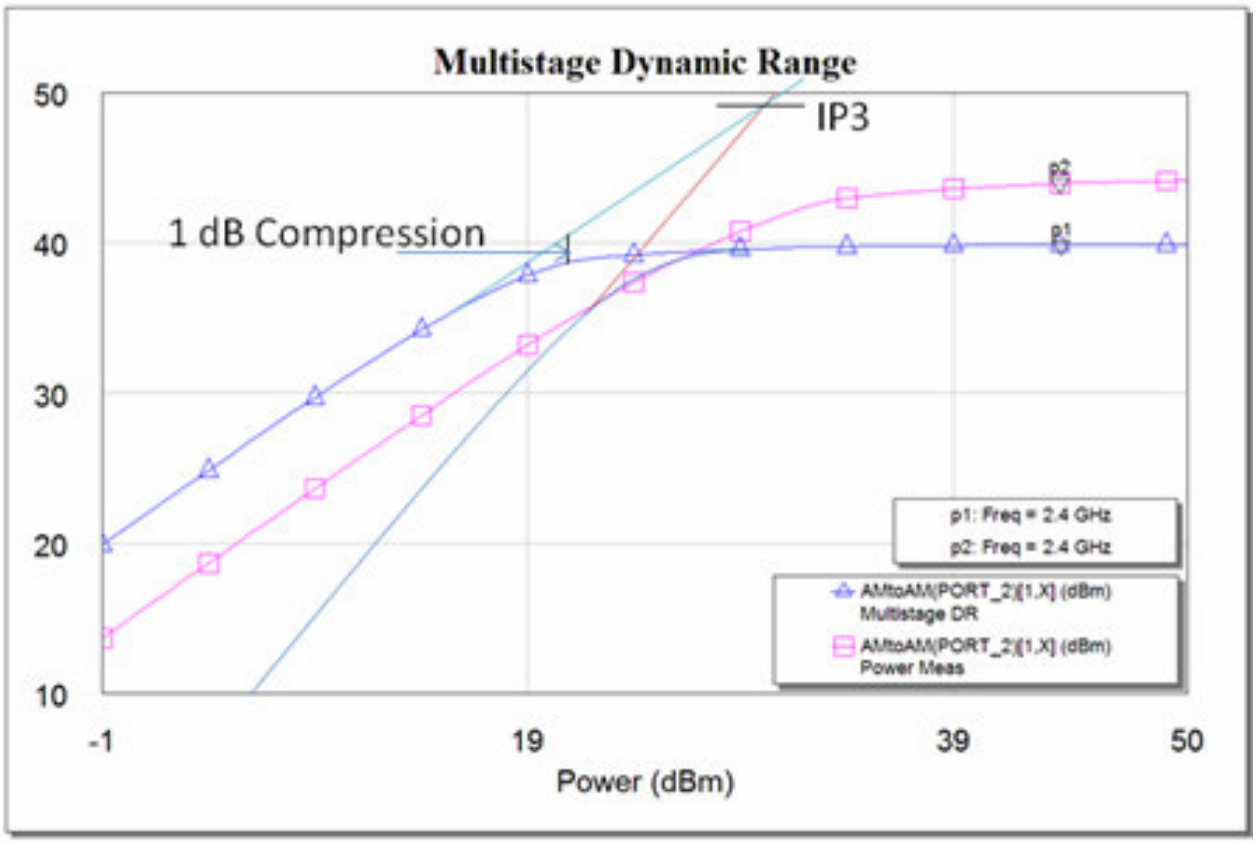

Figure 19. Upper range of two stage amplifier.

The upper range of the two stage amplifier is shown in Figure 19 with 1dBm compression and IP3. As discussed previously, the rule of thumb for the upper limit is 10 dBm below the IP3 point. This means the third order response, fifth order response, etc., are negligible and will not contribute into the output power. In this two stage amplifier, the 1 dBm and IP3 follows the rule thumb, and again, assuming the same noise floor as previously, the dynamic range is 99 dBm. Note, IP3 is an approximate curve. Comparing with the single stage amplifier, as shown in the pink curve, the linear region is shifted up but falls off faster at the upper limit. This results in a minimum 2 dB compression from the single stage as expected.

Conclusion:

In this paper, we have successfully simulated two microwave amplifier designs, the single stage amplifier, and the two stage amplifier. The simulated gain of our single stage amplifier at 2.4GHz is 14.3 dB with a return loss of 14.2dB. The tuned single stage amplifier gain, i.e. adjusting the matching network real-time, is 16.9dB. The two stage amplifier gain with tuned interfaced networks is 19.2 dB. Of which, all designs are in agreement with the transistor's specifications, i.e. nominal gain is 15.2 dB, minimum gain is 13 dB, and maximum gain of 17 dB.

Our amplifier has been shown to be stable through theoretical and simulated results. Even after increasing the drain bias current to a value above which the transistor could physically handle the simulated system remained stable.

A PCB design of our single stage amplifier has been provided, and could be fabricated in the future if anyone so desired. The main cost of the amplifier circuit would be the **Freescale MRF6S23140H** transistor which is around $100.

Appendix I

Freescale Semiconductor Document Number: MRF6S23140H [5]
Rev. 2, 12/2008

N-Channel Enhancement-Mode Lateral MOSFETs

2300-2400 MHz, 28 W AVG., 28 V
2 x W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 2300 to 2400 MHz. Suitable for WiMAX, WiBro and multicarrier amplifier applications. To be used in Class AB and Class C WLL applications

Typical 2- Carrier W-CDMA Performance: VDD = 28 Volts, IDQ = 1300 mA, Pout = 28 Watts Avg., f = 2390 MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
Power Gain — 15.2 dB
Drain Efficiency — 25%
IM3 @ 10 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
ACPR @ 5 MHz Offset — -40 dBc in 3.84 MHz Channel Bandwidth

Capable of Handling 10:1 VSWR, @ 32 Vdc, 2390 MHz, 140 Watts CW Output Power

Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	VDSS	-0.5, +68	Vdc
Gate-Source Voltage	VGS	-0.5, +12	Vdc

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (VDS = 68 Vdc, VGS = 0 Vdc)	IDSS	-	-	10	µAdc
Zero Gate Voltage Drain Leakage Current (VDS = 28 Vdc, VGS = 0 Vdc)	IDSS	-	-	1	µAdc
Gate-Source Leakage Current (VGS = 5 Vdc, VDS = 0 Vdc)	IGSS	-	-	500	nAdc
On Characteristics					
Gate Threshold Voltage (VDS = 10 Vdc, ID = 300 µAdc)	VGS(th)	1	2	3	Vdc

Gate Quiescent Voltage	VGS(Q)	2	2.8	4	Vdc	
(VDD = 28 Vdc, ID = 1300 mAdc, Measured in Functional Test)						
Drain-Source On-Voltage	VDS(on)	0.1	0.21	0.3	Vdc	
(VGS = 10 Vdc, ID = 3 Adc)						
Dynamic Characteristics	Crss	—	-	2	-	pF
Reverse Transfer Capacitance						
(VDS = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, VGS = 0 Vdc)						

Functional Tests (In Freescale Test Fixture, 50 ohm system) VDD = 28 Vdc, IDQ = 1300 mA, Pout = 28 W Avg., f = 2390 MHz, 2-Carrier
W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 measured in
3.84 MHz Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF

Power Gain	Gps	13	15.2	17	dB	
Drain Efficiency		ηD	23	25	-	%
Intermodulation Distortion	IM3	-	-37	-35	dBc	
Adjacent Channel Power Ratio		ACPR		-	-40	-38 dBc
Input Return Loss	IRL	-	-15	-	dB	

f(MHz)	Z_source	Z_load
2300	12.92 + j6.65	1.05 - j2.88
2310	13.06 + j6.73	1.04 - j2.82
2320	13.21 + j6.80	1.03 - j2.76
2330	13.37 + j6.87	1.01 - j2.70
2340	13.53 + j6.94	1.00 - j2.64
2350	13.70 + j7.01	0.99 - j2.58
2360	13.88 + j7.08	0.97 - j2.52
2370	14.06 + j7.14	0.96 - j2.46
2380	14.25 + j7.21	0.95 - j2.40
2390	14.45 + j7.27	0.94 - j2.34
2400	14.66 + j7.33	0.93 - j2.28

Zsource = Test circuit impedance as measured from gate to ground.
Zload = Test circuit impedance as measured from drain to ground.

Appendix II Parts List

Quantity	Designator	Footprint	Value	Mouser
2	C1, C2	0805	1nF	80-C0805C102K5R
2	C3, C4	0805	100nF	80-C0805C104K5R
1	L1	0805	1uH	80-L0805C1R0MPMST
1	L2	542-PM4301R0M-RC	1uH	542-PM43-1R0M-RC
1	Q1	MRF6S23140		841-MRF6S23140HR3

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