San José State University Department of Aviation & Technology Tech 62, Analog Circuits, Section 2, Fall 2017

Course and Contact Information

Instructor:	Dr. Mostafa Mortezaie
Office Location:	E103
Telephone:	(408) 306-1919
Email:	mostafamortezaie@yahoo.com, and CANVAS (preferred)
Office Hours:	TTh: 14:00-15:00
Class Days/Time:	TTh: 15:00-15:50
Classroom:	E103
Prerequisites:	TECH 060 and MATH 071 or MATH 030

Course Format:

The course relies on lecture materials presented in class and students are strongly encouraged to attend.

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on my faculty web page at http://www.sjsu.edu/people/firstname.lastname and/or on <u>Canvas Leaning Management System</u> course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through <u>MySJSU</u> at http://my.sjsu.edu (or other communication system as indicated by the instructor) to learn of any updates

Course Description

Semiconductor theory; p-n junction, bipolar transistors, JFETs and MOSFETs, optoelectronic devices. Operational amplifiers and 555 timers. Device applications: comparators, signal generators, active filters, in*strumentation amplifiers*, voltage regulators and power supplies. Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- 1. Describe the fundamentals of semiconductor diodes, transistors, op-amps, timers, and oscillators.
- 2. Build, identify, and analyze diode circuits, transistor circuits, op-amp circuits, active filters, and oscillators.
- 3. Design or modify fundamental electronic circuits to meet certain requirements

Required Texts/Readings

Textbook

Floyd, Thomas L. (2012). Electronic Devices. Conventional Current Version. 10th Ed. Upper Saddle River, NJ: Prentice Hall. ISBN-13: 978-0-13-441454-6.

Analog Circuits, Tech 62, Fall 2017

Page 1 of 8

You may obtain an electronic version at: http://www.mypearsonstore.com/bookstore/electronic-devices-conventional-current-version-subscription-9780134414546?xid=PSED

Other Readings

Instructor lecture notes and datasheets. For LTspice Exercises, download from the Link: https://media.pearsoncmg.com/ph/chet/careersresources/resourcessite/products/series.html#series,series=Electro nics and Electricity Technology

Course Requirements and Assignments

Class Participation

Students working in groups of 2-3 will solve Problems Sets (assigned problems from each chapter) posted on Canvas (https://sjsu.instructure.com). Click on the **Modules** tab. You need to include the question and the answer. The answers should be easy to follow. The whole class will check/discuss if the answers are correct before submitting them. This group discussion will reinforce and/or enhance your analog circuits' knowledge.

When the Group has determined that their answers are correct then each Group will submit their answers via Canvas (https://sjsu.instructure.com). **One report per group**. Click on the **Assignments** tab for submission. **Only the students whose names are indicated on the group report will get the credit.**

Class Participation contributes to CLOs 2 and 3, learning the fundamental concepts of analog circuits, developing teamwork skills and discussing the course material. Class Participation must be submitted by the due date indicated on the green sheet and has a weight of 10% of the final grade. You online inputs in the class will be used to assess objectively your class participation. Classes missed without approved reason and not made up will deduct from this score.

Lab experiments

You will complete lab assignments individually using the SPICE software. In addition, you will hardware 4 lab experiments and will compare the measurements obtained using real instruments with the ones obtained using SPICE. The written reports will be submitted one week after the date of the assigned lab. Lab experiments contribute to CLOs 2, 4 and 5, reinforcing the course material and developing teamwork skills. Lab experiments have a weight of 0.30% of the final grade.

Tests

You will take weekly take-home quizzes, two midterms and the final exam. Tests will start and end at the scheduled time. These tests contribute to CLOs 1, 2 and 3 as well as reinforcing the learning of the fundamental concepts of analog circuits. The weight of the tests for the final grade is 20% for the weekly quizzes, 20% for midterms and 20% for the final exam.

Weekly Take-home Quizzes

You will download the weekly take-home Quizzes posted on Canvas (https://sjsu.instructure.com). Click on the **Modules** tab. **You can work in groups** but **each student must submit his/her own quiz** via Canvas (https://sjsu.instructure.com) on or before the due date. Click on the **Assignments** tab.

Final Examination or Evaluation

Final Exam will be taken Thursday, 2017 December 14, 1445-1700.

Grading Information

Weekly online Quizzes, midterms and final exam will be graded based on the followed process and accurate answers. Class Participation will be evaluated based on the followed process and percent of accurate responses

Analog Circuits, Tech 62, Fall 2017

Page 2 of 8

provided. Lab experiments grade will be determined on the percent of lab assignments completed on or before the due date.

Determination of Grades

Grades will be determined based on your performance in Lab experiments, Class Participation, Weekly Quizzes, Midterms and Final Exam. The final grade for the course will be based on the following items and weights:

1.	Lab experiments	30%
2.	Class participation online	10%
3.	Weekly Quizzes	20%
4.	Midterms (2x10%)	20% (Midterm 1: October 10 th and Midterm 2 : Nov 16 th)

5. Final Exam 20% (Final Exam: December 14th)

There will be no curving of grades. Final grades will be assigned as follows:

А	>94	A-	90-93	
B+	85-89	В	80-84	B- 76-79
C+	72-75	С	69-71	C- 65-68
D+	62-64	D	59-61	D- 56-58
F	<55			

Classroom Protocol

- 1. You are expected to attend all meetings for the course as you are responsible for material discussed therein, and active participation is frequently essential to ensure maximum benefit to all class members. Attendance is fundamental to course objectives; for example, you may be required to interact with others in the class.
- 2. Download (DO NOT print) read and bring softcopies of the assigned Chapter handout 2017 posted on Canvas (https://sjsu.instructure.com). Click on the **Modules** tab.
- 3. You will study the assigned chapter/material before coming to lecture by watching the assigned videos, reading the textbook and reviewing the PowerPoint presentation posted on Canvas (https://sjsu.instructure.com). Click on the Modules tab.
- 4. After reviewing the chapter materials you will answer the Problem Sets (assigned problems at the end of the chapter) posted on Canvas (https://sjsu.instructure.com). Click on the **Modules** tab.
- 5. Instructor will explain key points and answer questions from students. Instructor may add related material to enrich the course content.
- 6. Instructor will become more as a facilitator of learning. This means that the instructor will provide as much individual or group assistance as needed.
- 7. Students should work and learn in teams. This is very important to be successful in the real world.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

Commented [P1]: This grading scale seems too low. F less than

Analog Circuits, Tech 62, Fall 2017

Page 3 of 8

Tech 62 Analog Circuits, Fall 2017 Course Schedule

The schedule is subject to change with one week notice on CANVAS and email.

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	Aug 24	Introduction/Orientation/Greensheet
1	-	Email Proof of completion of course prereq (Tech 60 or equivalent and MATH 71 or
		MATH 30) by 8/29
		Download (DO NOT print) read and bring softcopies of Chapters 1 & 2 handout 2017
		from Canvas. Modules tab.
		Read Ch1: Introduction to Electronics/ Ch 2: Diodes
		Watch video: http://www.youtube.com/watch?v=lA6V205VMyY
		Read 1-4: The PN junction
		Read 2-1: Diode Operation
		Kead 2-5: Diode Models
		DOAD LISPICE: Set up for LAB
		Frepare in davance for the next session. Download (DO NOT print) read and bring softenning of Chapter 4 handout 2017 from
		Conves
		Modules tab
		Watch video: http://www.voutube.com/watch?v=-td7YT-Pums&feature=related
		Read Chapter 4:
		4-1: BJT Structure
		4-2: Basic BJT Operation
		4-3: BJT Characteristics And Parameters
		Answer Problems Set 1
2	Aug 29, 31	Discuss Chapter 4
_		Email Proof of completion of course prereq (Tech 60 or equivalent and MATH 71 or
		MATH 30) by 8/29
		4-4: The BJT As An Amplifier
		4-5: The BJT As A Switch
		Prepare Quiz Set1
		• Submit Weekly Quiz I via Canvas when available
		Due by 11:00 pm on 0/11
		Prenare in advance for the next session:
		Chapter 4-5 handout 2017 from Canvas or email
		Watch video: https://www.voutube.com/watch?v=WLYc6oD2BYA
		Read:
		5-1: The DC Operating Point
		5-2: Voltage Divider Bias
		5-3: Emitter, Base, Emitter-Feedback And Collector-Feedback Biasing
		Finish Assignment Set 1
3	Sep 5, 7	Discuss Chapter 5
-		Finish Problems Set 2
		Submit Problems Set 1 via Canvas. Click on the Assignments tab. Due by 11:00 pm
		on 9/13! Group submission. Only the indicated students will get the credit.
		Submit Weekly Quiz 2 via Canvas. Click on the Assignments tab. Due by 11:00 pm on
		9/13! Individual submission
		Prepare in advance for the next session:

Analog Circuits, Tech 62, Fall 2017

Page 4 of 8

Week	Date	Topics, Readings, Assignments, Deadlines
		Download (DO NOT print) read and bring softcopies of Chapter 6 handout 2017 from Canvas. Modules tab. Read 6-1: Amplifier Operation Watch video: http://www.youtube.com/watch?v=-LPALAwcYkg Read 6-2: Transistor AC Models Watch video: https://www.youtube.com/watch?v=Pkjn18Ekjic Read 6-3: The Common-Emitter Amplifier Read 6-4: The Common-Collector Amplifier Answer Problems Set 3
4,5	Sep 12, 14, 19	Discuss Chapter 6 Finish Problems Set 3 Submit Problems Set 2 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> on 9/22! Group submission. Only the indicated students will get the credit. Submit Weekly Quiz 3 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm on</i> 9/22! Individual submission Read and bring Chapter 6 handout 2017 from Canvas. Modules tab. Read in advance for the next session: 6-5: The Common-Base Amplifier 6-6: Multistage Amplifiers
5,6	Sep 21, 26	Answer Problems Set 4 Discuss Chapter 6 Finish Problems Set 3 via Canvas, Click on the Assignments tab. Due by 11:00 pm on 9/29! Group submission. Only the indicated students will get the credit. Submit Weekly Quiz 4 via Canvas.) Click on the Assignments tab. Due by 11:00 pm on 9/29! Individual submission Prepare in advance for the next session: Download (DO NOT print) read and bring softcopies of Chapter 8 handout 2017 from Canvas. Modules tab. Read 8-1: The JFET Watch video: http://www.youtube.com/watch?v=BzsXNhigVC0 Read 8-2: JFET Characteristic and Parameters Read 8-4: The Ohmic Region Answer Problems Set 5
6,7	Sep 28, Oct 3	Discuss Chapter 8 Finish Problems Set 5 Submit Problems Set 4 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm on 10/6! Group submission</i> . Only the indicated students will get the credit. Submit Weekly Quiz 5 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm on 10/6! Individual submission</i> Prepare for Midterm 1 You can use schematic diagrams and equations only. No text is allowed such as If resistor shorts it is 0, etc.

Analog Circuits, Tech 62, Fall 2017

Page 5 of 8

Week	Date	Topics, Readings, Assignments, Deadlines
7	Oct 5	Review Q & A
8	Oct 10	Midterm 1 Prepare in advance for the next session: Download (DO NOT print) read and bring softcopies of Chapter 9 handout 2017 from Canvas. Modules tab. Read 9-1: The Common-Source Amplifier Read 9-2: The Common-Drain Amplifier Read 9-3: The Common-Gate Amplifier Answer Problems Set 6
9,10	Oct 12, 17	Discuss Chapter 10 Finish Problems Set 7 Submit Problems Set 6 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> on 11/1! Group submission. Only the indicated students will get the credit. Submit Weekly Quiz 7 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm on</i> 11/1! Individual submission Download (DO NOT print) read and bring softcopies of Chapter 12 handout 2017 from Canvas. Modules tab Prepare in advance for the next session: Watch video: http://www.youtube.com/watch?v=TQB1VILBgJE Read 12-4: Op-Amps with Negative Feedback Read 12-5: Effects of Negative Feedback on Op-Amp Impedance Read 12-7: Open-Loop Response Read 12-8: Closed-Loop Response Answer Problems Set 8
10,11	Oct 19, 24	Discuss Chapter 12 Finish Problems Set 8 Submit Problems Set 7 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> on 11/8! Group submission. Only the indicated students will get the credit. Submit Weekly Quiz 8 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm on</i> 11/8! Individual submission Download (DO NOT print) read and bring softcopies of Chapters 13 & 16 handout 2017 from Canvas. Modules tab Prepare in advance for the next session: Watch video: http://www.youtube.com/watch?v=nG8gA_kAp-Y Read 13-1: Comparators Read 13-2: Summing Amplifiers Read 13-3: Integrators and Differentiators Read 16-2: Feedback Oscillator Principles and Oscillator types Answer Problems Set 9
11,12, 13	Oct 26, Nov 2, 7, 9	Discuss Chapters 13 & 16 Finish Problems Set 9 Submit Problems Set 8 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> on 11/22! Group submission. Only the indicated students will get the credit.

Analog Circuits, Tech 62, Fall 2017

Page 6 of 8

Week	Date	Topics, Readings, Assignments, Deadlines
		Submit Weekly Quiz 9 via Canvas. Click on the Assignments tab. Due by 11:00 pm on 11/22! Individual submission Prepare in advance for the next session: Watch video: http://www.youtube.com/watch?v=yj4uVVV5Nsg Read 2-4: Half-Wave Rectifiers Read 2-5: Full-Wave Rectifiers Answer Problems Set 10
14	Nov14	Review Q & A Finish Problems Set 10 Submit Problems Set 9 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> <i>on 11/29! Group submission</i> . Only the indicated students will get the credit. Submit Weekly Quiz 10 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> <i>on 11/29! Individual submission</i>
14	Nov 16	Prepare for Midterm 2 Midterm 2 Prepare in advance for the next session: Download (DO NOT print) read and bring softcopies of Chapter 3 handout 2017 from Canvas. Modules tab Read 2-6: Power Supply Filters and Regulators Read Ch3: Special-Purpose Diodes Watch video: http://www.youtube.com/watch?v=jG2YAtTWxvc Read 3-1: The Zener Diode Read 3-2: Zener Diode Application Answer Problems Set 11
15	Nov 21	Thanking Chapters 1 – 16 Learnings
16	Nov 28, 30	Discuss Chapter 3 and others Finish Problems Set 11
17	Dec 5, 7	Review All material Submit Problems Set 10 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> <i>on 12/13! Group submission</i> . Only the indicated students will get the credit . Submit Problems Set 11 via Canvas. Click on the Assignments tab. <i>Due by 11:00 pm</i> <i>on 12/13! Group submission</i> . Only the indicated students will get the credit . Prepare for FINAL
Final Exam	Thursday, 2017 Dec14,	Venue TBD 14:45-17:00.

Analog Circuits, Tech 62, Fall 2017

SAN JOSE STATE UNIVERSITY

Department of Aviation & Technology

Tech 62 Labs @ IS117		
Fall 2017		
Section	M 9:00-11:15	
Section	F 9:00 - 11:15	

Section F $9:00 - 11:15$	by Appointment in Lat
Your Week Friday/Monday	Lab Experiments
(dates subject to revision)	
1	Hands On, Lab Safety and Rules by TAs. SPICE Introduction.
(Aug 25/28)	
1&2	SPICE Bipolar Transistor characteristics. Refer Experiment #11
(Sep 1&8 / Sep 11&18)	
1&2	SPICE Collector-feedback biased BJT. Refer Experiment #16
(Sep 1&8 / Sep 11&18)	
2&3	#1 Hardwired lab Experiment
(Sep 8 &15 / Sep 18 & 25)	Collector-feedback biased BJT (2N3904 or equivalent)
	BONUS: Bipolar Transistor characteristics
3&4	SPICE Voltage Divider Biased BJT. Refer Experiment #13
(Sep 15&22/ Sep 25&Oct 2)	
4&5	#2 Hardwired Lab Experiment
(Sep 22&29 / Oct 2 & 9)	Voltage Divider Biased BJT
6	SPICE Small-signal common-emitter amplifier. Refer Experiment #17
(Oct 6/Oct 16)	
6&7	#3 Hardwired Lab Experiment
(Oct 6&13/ Oct 16&23)	Small-signal common-emitter amplifier
8	SPICE JFET Small-signal common-source amplifier. Refer Experiment
(Oct 20 / Oct 30)	#27
8&9	SPICE OPAMP Inverting voltage amplifier. Refer Experiment #32
(Oct 20&27 / Oct 30&Nov 6)	SPICE OPAMP Non Inverting voltage amplifier. Refer Experiment #31
10 (Nov 3 / Nov 13)	catch up - 11/10/2017 Veterans Day – Campus Closed
10&11	#4 Hardwired Lab Experiment
(Nov 3&17 / Nov 13&20)	Inverting Voltage Amplifier
12 (Nov 22-24)	Thanksgiving Holidays – Campus Closed
13/12	SPICE Op-amp Integrator and Differentiator. Refer Experiment #35.
(Nov 30/Nov 20 & 27)	
14/13	Catch up
(Dec 8 / Dec 4)	BONUS: Hardwire Op-amp Integrator or Differentiator

Notes:

1. Each student will perform all lab experiments using SPICE: <u>Simulation Program with Integrated Circuit Emphasis</u> (LTspice/Multisim software).

2. Each student will submit an online lab report a week after the lab is completed.

3. Students working in groups of 2-3 members will hardwire four lab experiments. The measurements obtained in these hardwired lab experiments will be compared with the ones obtained using SPICE.

4. While one batch of students work at the Computer Area other half will work on the instrument test benches area. Simulation and Hardwiring may be repeated in any order.

5. Each group will submit a report online of each hardwired lab within week after the lab is completed.

6. Experiment is complete when Report is complete and accepted. If you have finished the Lab data collection you may spend the rest of the time in Lab to complete the report and submit online.

Analog Circuits, Tech 62, Fall 2017

Page 8 of 8

Dr. Ignatius Bezzam

Office Hour: MF 1100:12

TAs: ali.saeidiashtiyani@sjsu, melody.teoh@sjsu.edu